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DATA SHEET

PCF2113x
LCD controllers/drivers

Product specification
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Philips
Semiconductors

PHILIPS

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1 FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5×7 character format plus cursor; 5×8 for kana (Japanese) and user defined symbols
- Icon mode: reduced current consumption while displaying
- Icon blink function
- On-chip:
  - Configurable 4, 3 or 2 voltage multiplier generating LCD supply voltage, independent of V_{DD}, programmable by instruction (external supply also possible)
  - Temperature compensation of on-chip generated V_{LCD}: −0.16 to −0.24 %/K (programmable by instruction)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- Display data RAM: 80 characters
- Character generator ROM: 240, 5×8 characters
- Character generator RAM: 16, 5×8 characters; 3 characters used to drive 120 icons, 6 characters used if icon blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I^2C-bus interface
- CMOS compatible
- 18 row and 60 column outputs
- Multiplex rates 1 : 18 (for normal operation), 1 : 9 (for single line operation) and 1 : 2 (for icon only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range $V_{DD1} - V_{SS1}$ = 1.8 to 5.5 V (chip may be driven with two battery cells)
- V_{LCD} generator supply voltage range $V_{DD2} - V_{SS2}$ = 2.2 to 4.0 V
- Display supply voltage range $V_{LCD} - V_{SS2}$ = 2.2 to 6.5 V
- Direct mode to save current consumption for icon mode and Mux 1 : 9 (depending on V_{DD2} value and LCD liquid properties)
- Very low current consumption (20 to 200 μA):
  - Icon mode: <25 μA
  - Power-down mode: <2 μA.

1.1 Note

Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2113x is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2-line by 12 or 1-line by 24 characters with 5×8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2113x interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I^2C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'x' in PCF2113x characterizes the built-in character set. Various character sets can be manufactured on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2113AU/10/F4	–	chip on flexible film carrier	–
PCF2113DU/10/F4	–	chip on flexible film carrier	–
PCF2113DU/F4	–	chip in tray	–
PCF2113DH/F4	LQFP100	plastic low profile quad flat package; 100 leads; body $14 \times 14 \times 1.4$ mm	SOT407-1
PCF2113DU/2/F4	–	chip with bumps in tray	–
PCF2113EU/2/F4	–	chip with bumps in tray	–
PCF2113WU/2/F4	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

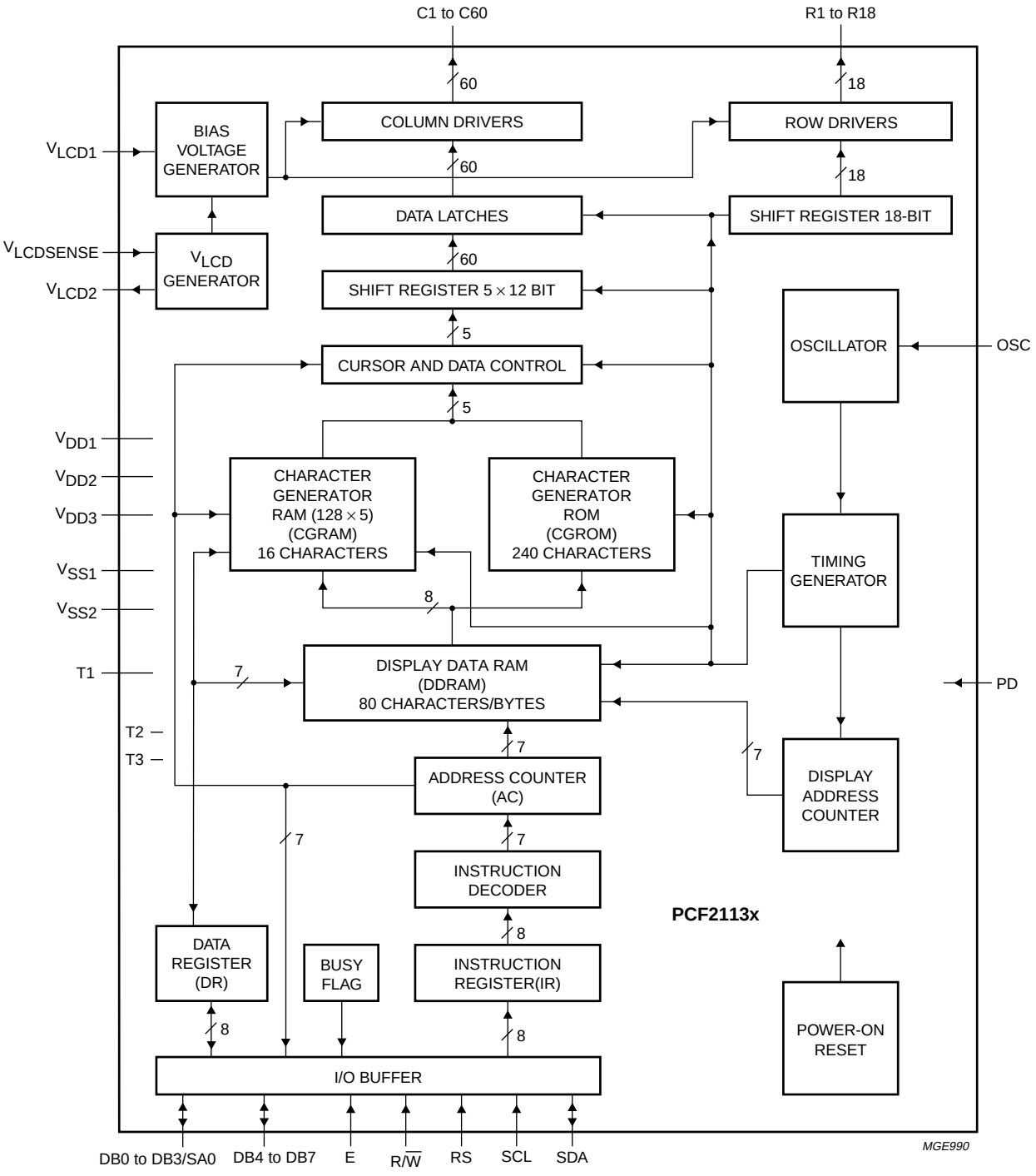


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN PCF2113DH	PAD[1] PCF2113XU	TYPE	DESCRIPTION
V_{DD1}	1	1	P	supply voltage 1 for all except V_{LCD} generator
OSC	2	2	I	oscillator/external clock input; note 2
PD	3	3	I	power-down select input; for normal operation PD is LOW
T3	–	4	I	test pad; open circuit and not user accessible
T1	4	5	I	test pin; must be connected to V_{SS1}
T2	–	6	I	test pad; must be connected to V_{SS1}
V_{SS1}	5	7	P	ground 1 for all except V_{LCD} generator
V_{SS2}	6	8	P	ground 2 for V_{LCD} generator
V_{LCD2}	7	9	O	V_{LCD} output if V_{LCD} is generated internally; note 7
$V_{LCDSENSE}$	–	10	I	input (V_{LCD}) for voltage multiplier regulation; notes 3 and 7
V_{LCD1}	8	11	I	input for generation of LCD bias levels; note 7
R9 to R16	9 to 16	12 to 19	O	LCD row driver outputs 9 to 16
R18	17	20	O	LCD row driver output 18
C60 to C53	18 to 25	21 to 28	O	LCD column driver outputs 60 to 53
dummy pad	–	29	–	
dummy pad	–	30	–	
C52 to C28	26 to 50	31 to 55	O	LCD column driver outputs 52 to 28
dummy pad	–	56	–	
dummy pad	–	57	–	
C27 to C3	51 to 75	58 to 82	O	LCD column driver outputs 27 to 3
dummy pad	–	83	–	
dummy pad	–	84	–	
C2	76	85	O	LCD column driver output 2
C1	77	86	O	LCD column driver output 1
R8 to R1	78 to 85	87 to 94	O	LCD row driver outputs 8 to 1
R17	86	95	O	LCD row driver output 17
SCL	87	96	I	I^2C-bus serial clock input; note 4
SDA	88	97	I/O	I^2C-bus serial data input/output; note 4
E	89	98	I	data bus clock input; note 4
RS	90	99	I	register select input
R/$\overline{W}$	91	100	I	read/write input
DB7	92	101	I/O	8-bit bidirectional data bus bit 7; note 5
DB6	93	102	I/O	8-bit bidirectional data bus bit 6
DB5	94	103	I/O	8-bit bidirectional data bus bit 5
DB4	95	104	I/O	8-bit bidirectional data bus bit 4
DB3/SA0	96	105	I/O	8-bit bidirectional data bus bit 3 or I^2C-bus address pin; notes 4 and 5
DB2	97	106	I/O	8-bit bidirectional data bus bit 2
DB1	98	107	I/O	8-bit bidirectional data bus bit 1

SYMBOL	PIN PCF2113DH	PAD(1) PCF2113XU	TYPE	DESCRIPTION
DB0	99	108	I/O	8-bit bidirectional data bus bit 0
V_{DD2}	100	109	P	supply voltage 2 for V_{LCD} generator; note 6
V_{DD3}	–	110	P	supply voltage 3 for V_{LCD} generator; notes 3 and 6

Notes

1. Bonding pad location information is given in Chapter 17.
2. When the on-chip oscillator is used this pad must be connected to V_{DD1}.
3. In the LQFP100 version this signal is connected internally and can not be accessed at any pin.
4. When the I^2C-bus is used, the parallel interface pin E must be LOW. In the I^2C-bus read mode DB7 to DB0 should be connected to V_{DD1} or left open-circuit.
   When the parallel bus is used, the pins SCL and SDA must be connected to V_{SS1} or V_{DD1}; they must not be left open-circuit.
   When the 4-bit interface is used without reading out from the PCF2113x (R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB4 can either be set to V_{SS1} or V_{DD1} instead of leaving them open-circuit.
5. DB7 may be used as the busy flag, signalling that internal operations are not yet completed. In 4-bit operations the four higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit except for I^2C-bus operations (see note 4).
6. V_{DD2} and V_{DD3} should always be equal.
7. When V_{LCD} is generated internally, pins V_{LCD1}, V_{LCD2} and $V_{LCDSENSE}$ must be connected together. When external V_{LCD} is supplied, pin V_{LCD2} should be left open-circuit to avoid any stray current, pins V_{LCD1} and $V_{LCDSENSE}$ must be connected together.

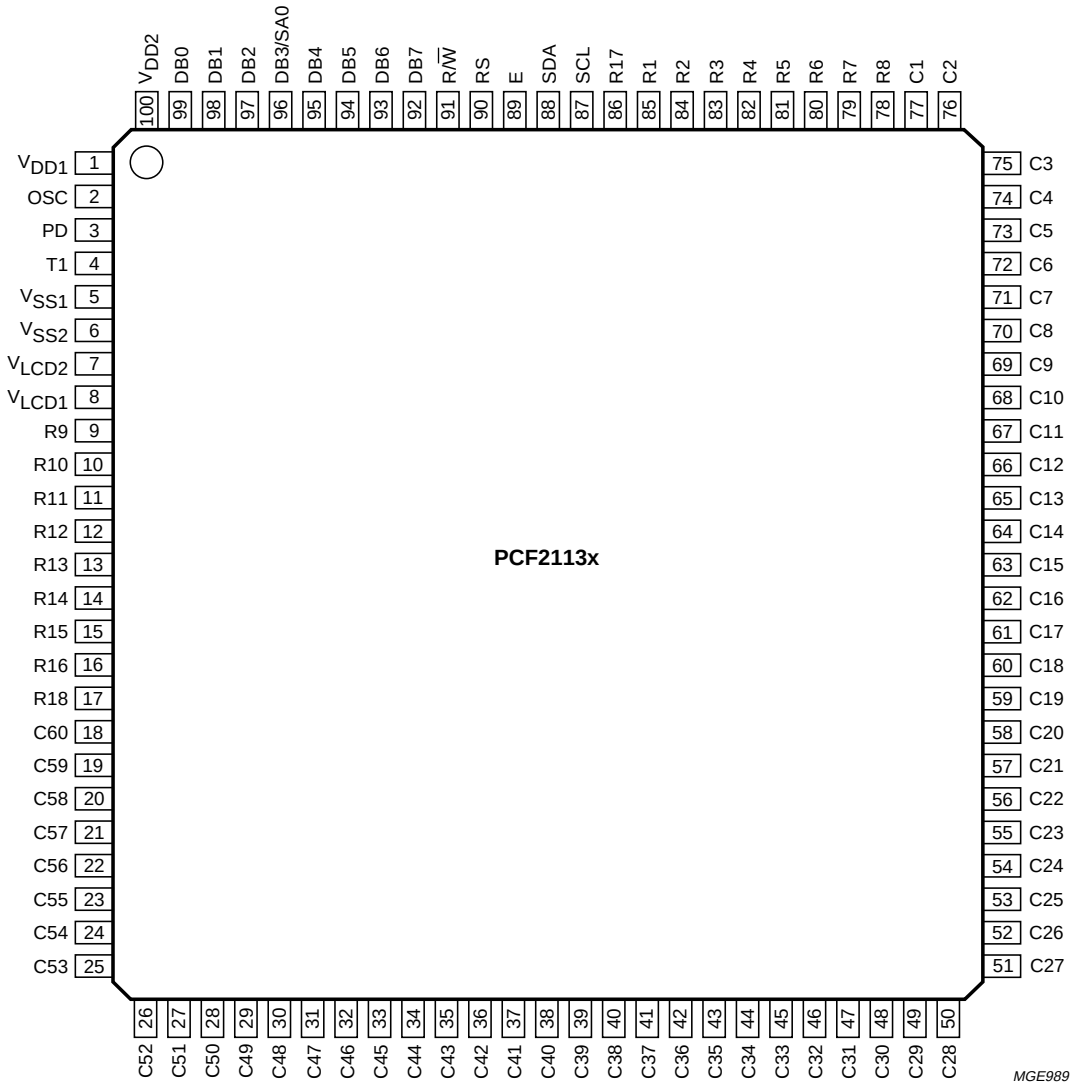


Fig.2 Pin configuration (LQFP100).

7 FUNCTIONAL DESCRIPTION

7.1 LCD supply voltage generator

The LCD supply voltage may be generated on-chip. The V_{LCD} generator is controlled by two internal 6-bit registers: V_A and V_B. The nominal LCD operating voltage at room temperature is given by the relationship:

$V_{OP(nom)}$ = (integer value of register $\times$ 0.08) + 1.82

7.1.1 PROGRAMMING RANGES

Programmed value: 1 to 63. Voltage: 1.90 to 6.86 V. T_{ref} = 27 °C.

Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the V_{LCD} tolerance and temperature coefficient must be taken into account.

Values below 2.2 V are below the specified operating range of the chip and are therefore not allowed.

Value 0 for V_A and V_B switches the generator off (i.e. V_A = 0 in character mode, V_B = 0 in icon mode).

Usually register V_A is programmed with the voltage for character mode and register V_B with the voltage for icon mode.

When V_{LCD} is generated on-chip the V_{LCD} pins should be decoupled to V_{SS} with a suitable capacitor.

The generated V_{LCD} is independent of V_{DD} and is temperature compensated. When the V_{LCD} generator and the direct mode are switched off, an external voltage may be supplied at connected pins V_{LCD1} and V_{LCD2}. V_{LCD1} and V_{LCD2} may be higher or lower than V_{DD2}.

During direct mode (program DM register bit) the internal V_{LCD} generator is turned off and the V_{LCD2} output voltage is directly connected to V_{DD2}. This reduces the current consumption during icon mode and Mux 1 : 9 (depending on V_{DD2} value and LCD liquid properties).

The V_{LCD} generator ensures that, as long as V_{DD} is in the valid range (2.2 to 4 V), the required peak voltage V_{OP} = 6.5 V can be generated at any time.

7.2 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels. Using a 5-level bias scheme for 1 : 18 maximum rate allows V_{LCD} < 5 V for most LCD liquids. The intermediate bias levels for the different multiplex rates are shown in Table 1. These bias levels are automatically set to the given values when switching to the corresponding multiplex rate.

Table 1 Bias levels as a function of multiplex rate; note 1

MULTIPLEX RATE	NUMBER OF LEVELS	V_1	V_2	V_3	V_4	V_5	V_6
1 : 18	5	V_{LCD}	$^3/_4$	$^1/_2$	$^1/_2$	$^1/_4$	V_{SS}
1 : 9	5	V_{LCD}	$^3/_4$	$^1/_2$	$^1/_2$	$^1/_4$	V_{SS}
1 : 2	4	V_{LCD}	$^2/_3$	$^2/_3$	$^1/_3$	$^1/_3$	V_{SS}

Note

1. The values in the table are given relative to $V_{LCD} - V_{SS}$, e.g. $^3/_4$ means $^3/_4 \times (V_{LCD} - V_{SS})$.

7.3 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pin must be connected to V_{DD1}.

7.4 External clock

If an external clock is to be used this input is at the OSC pin. The resulting display frame frequency is given by:

$$f_{frame} = \frac{f_{OSC}}{3072}$$

Only in the Power-down mode is the clock allowed to be stopped (OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state.

7.5 Power-on reset

The on-chip Power-on reset block initializes the chip after power-on or power failure. This is a synchronous reset and requires 3 oscillator cycles to be executed.

7.6 Power-down mode

The chip can be put into Power-down mode by applying an external active HIGH level to the PD pin. In Power-down mode all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to V_{SS}).

During power-down, information in the RAMs and the chip state are preserved. Instruction execution during power-down is possible when pin OSC is externally clocked.

7.7 Registers

The PCF2113x has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select (RS) signal determines which register will be accessed. The instruction register stores instruction codes such as ‘display clear’, ‘cursor shift’, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM).The instruction register can be written to but not read from by the system controller.

The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the ‘read data’ instruction.

7.8 Busy flag

The busy flag indicates the internal status of the PCF2113x. A logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output to pin DB7 when bit RS = 0 and bit R/$\overline{W}$ = 1. Instructions should only be written after checking that the busy flag is at logic 0 or waiting for the required number of cycles.

7.9 Address Counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands ‘set CGRAM address’ and ‘set DDRAM address’. After a read/write operation the address counter is automatically incremented or decremented by 1.
The address counter contents are output to the bus (DB6 to DB0) when bit RS = 0 and bit R/$\overline{W}$ = 1.

7.10 Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM to display addressing scheme is shown in Fig.3. With no display shift the characters represented by the codes in the first 24 RAM locations starting at address 00H in line 1 are displayed. Figures 4 and 5 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM, wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together.
The address ranges and wrap-around operations for the various modes are shown in Table 2.

Table 2 Address space and wrap-around operation

MODE	1 × 24	2 × 12	1 × 12
Address space	00 to 4F	00 to 27; 40 to 67	00 to 27
Read/write wrap-around (moves to next line)	4F to 00	27 to 40; 67 to 00	27 to 00
Display shift wrap-around (stays within line)	4F to 00	27 to 00; 67 to 40	27 to 00

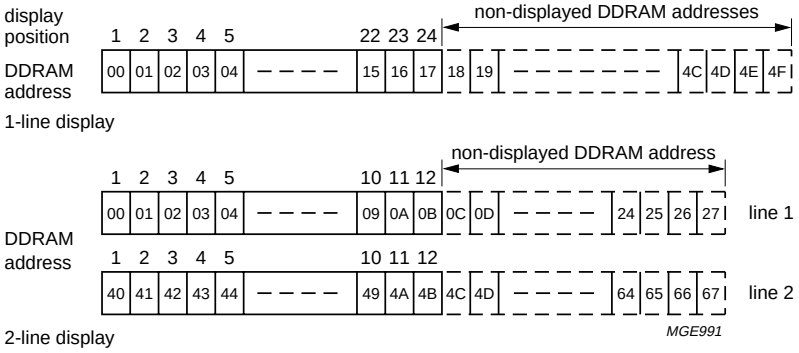

display position
1 2 3 4 5 22 23 24
non-displayed DDRAM addresses
DDRAM address
00 01 02 03 04 15 16 17 18 19 4C 4D 4E 4F
1-line display
non-displayed DDRAM address
1 2 3 4 5 10 11 12
00 01 02 03 04 09 0A 0B 0C 0D 24 25 26 27 line 1
DDRAM address
1 2 3 4 5 10 11 12
40 41 42 43 44 49 4A 4B 4C 4D 64 65 66 67 line 2
2-line display
MGE991

Fig.3 DDRAM to display mapping; no shift.

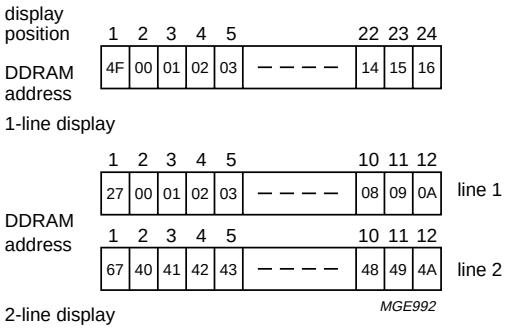


Fig.4 DDRAM to display mapping; right shift.

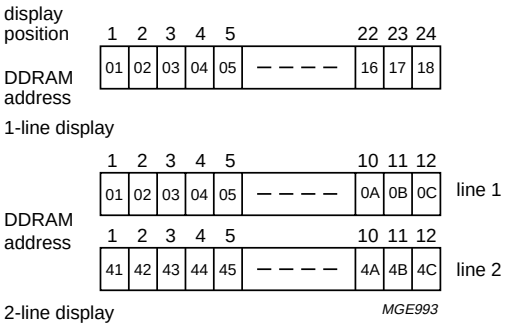


Fig.5 DDRAM to display mapping; left shift.

7.11 Character Generator ROM (CGROM)

The CGROM generates 240 character patterns in a 5×8 dot format from 8-bit character codes. Figures 7, 8, 9 and 10 show the character sets that are currently implemented.

7.12 Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the CGRAM. Some CGRAM characters (see Fig.16) are also used to drive icons (6 if icons blink and both icon rows are used in the application; 3 if no blink but both icon rows are used in the application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.7). Figure 11 shows the addressing principle for the CGRAM.

7.13 Cursor control circuit

The cursor control circuit generates the cursor underline and/or cursor blink as shown in Fig.6 at the DDRAM address contained in the address counter.

When the address counter contains the CGRAM address the cursor will be inhibited.

7.14 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

7.15 LCD row and column drivers

The PCF2113x contains 18 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 12, 13, 14 and 15 show typical waveforms. Unused outputs should be left unconnected.

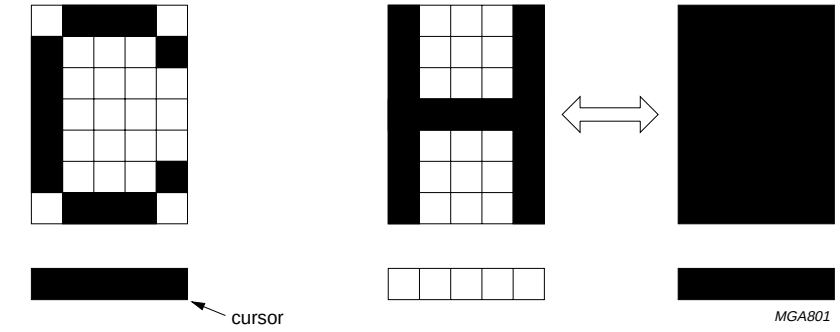


Fig.6 Cursor and blink display examples.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGE994

Fig.7 Character set ‘A’ in CGROM.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGD688

Fig.8 Character set ‘D’ in CGROM.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

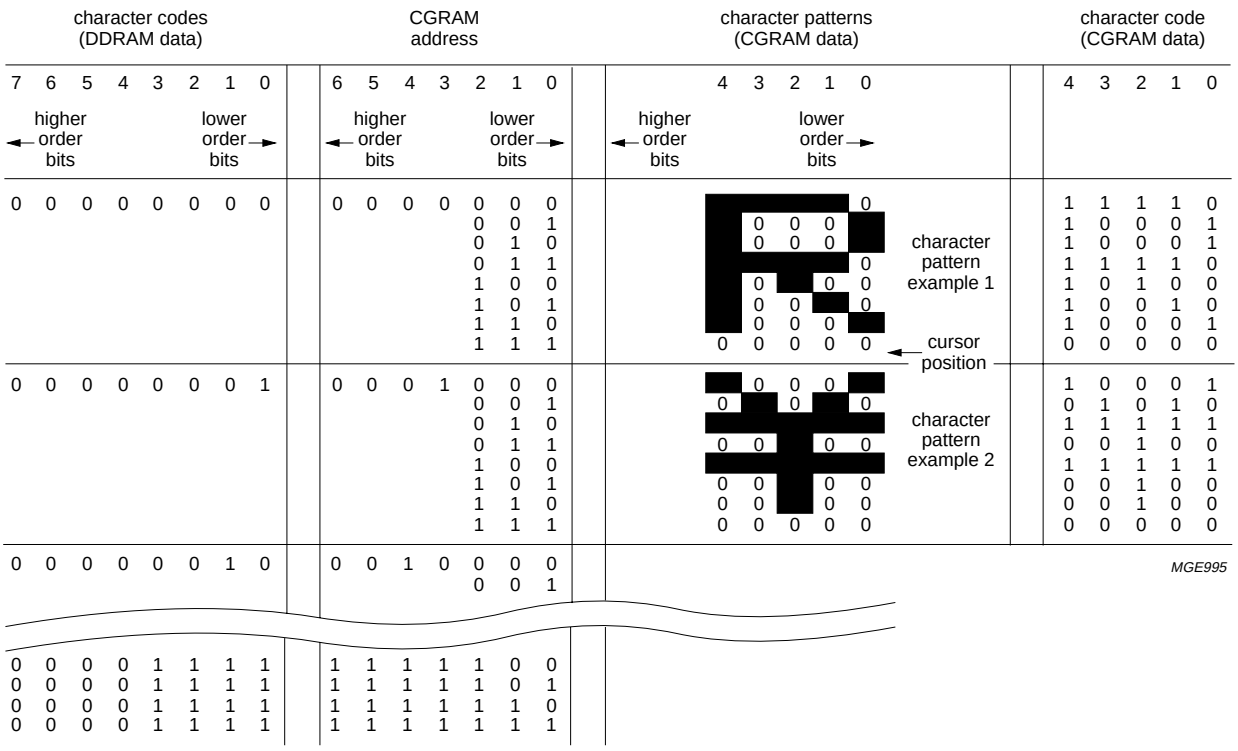
MGD689

Fig.9 Character set ‘E’ in CGROM.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

MGU204

Fig.10 Character set ‘W’ in CGROM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in this figure.

As shown in Figs 7 and 8, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the ‘set CGRAM address’ command. Bit 6 can be set using the ‘set DDRAM address’ command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the ‘read busy flag’ and ‘address counter’ command.

Fig.11 Relationship between CGRAM addresses, data and display patterns.

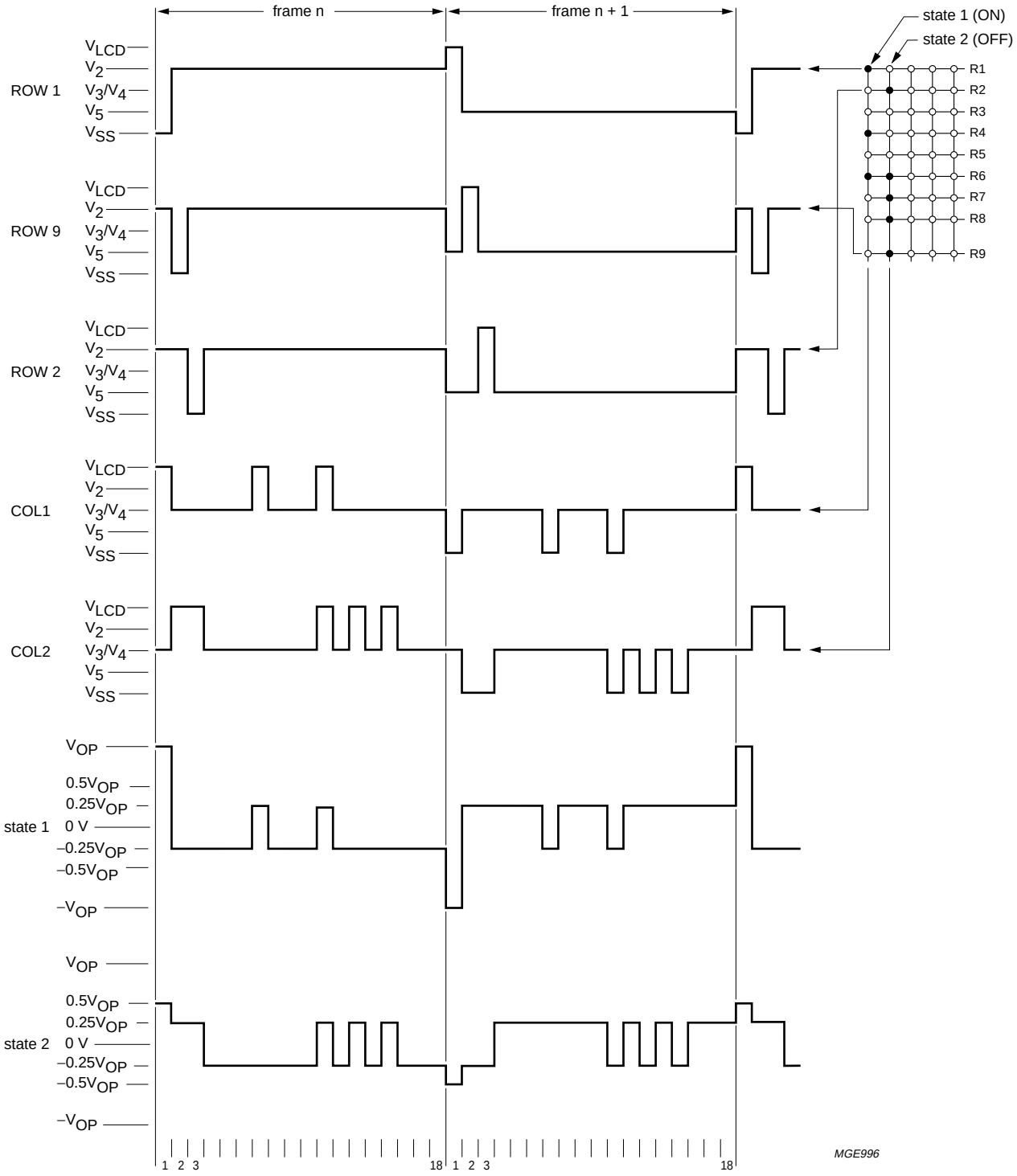
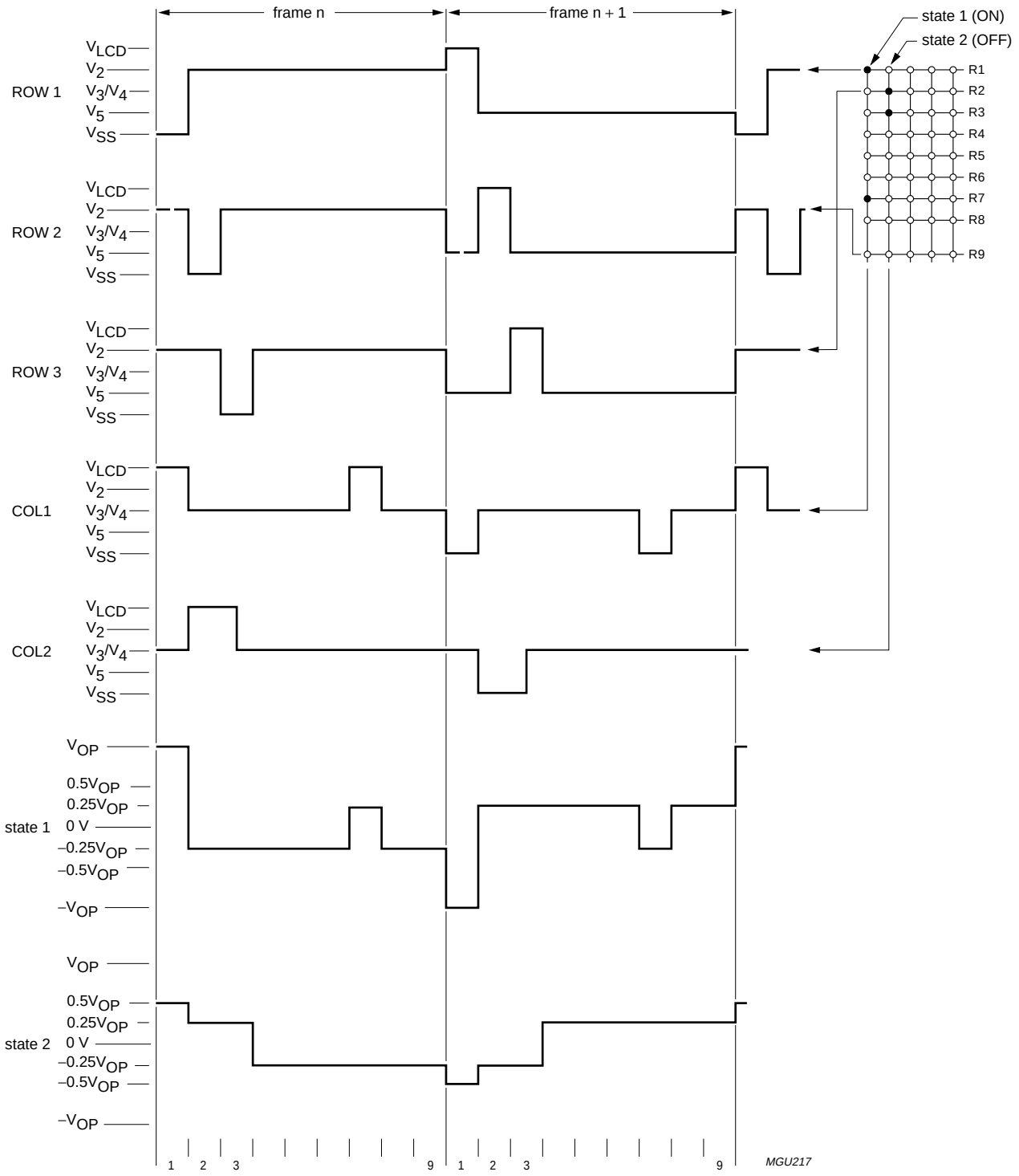


Fig.12 MUX 1 : 18 LCD waveforms; character mode.



R10 to R18 to be left open.

Fig.13 MUX 1 : 9 LCD waveforms; character mode.

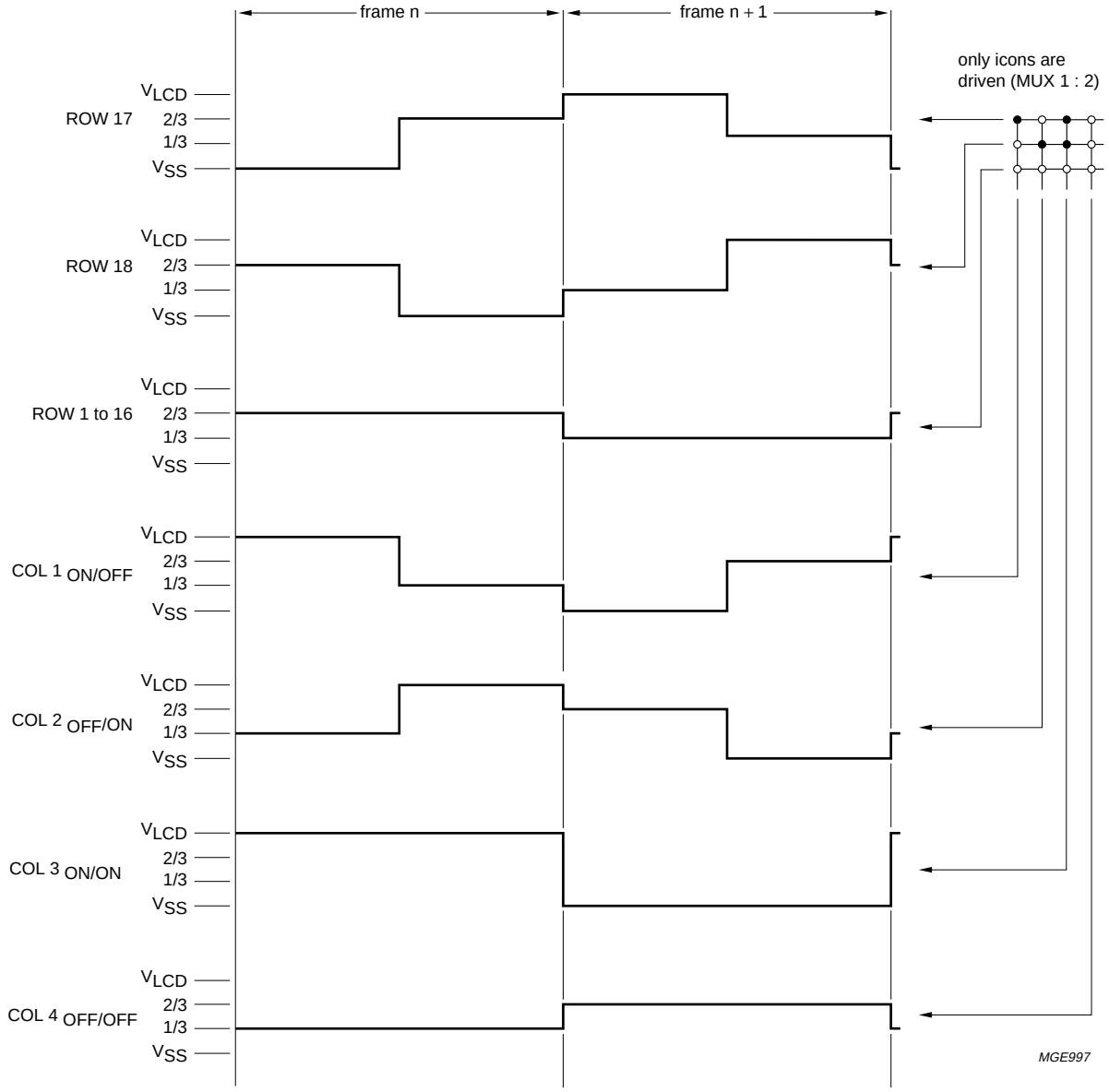
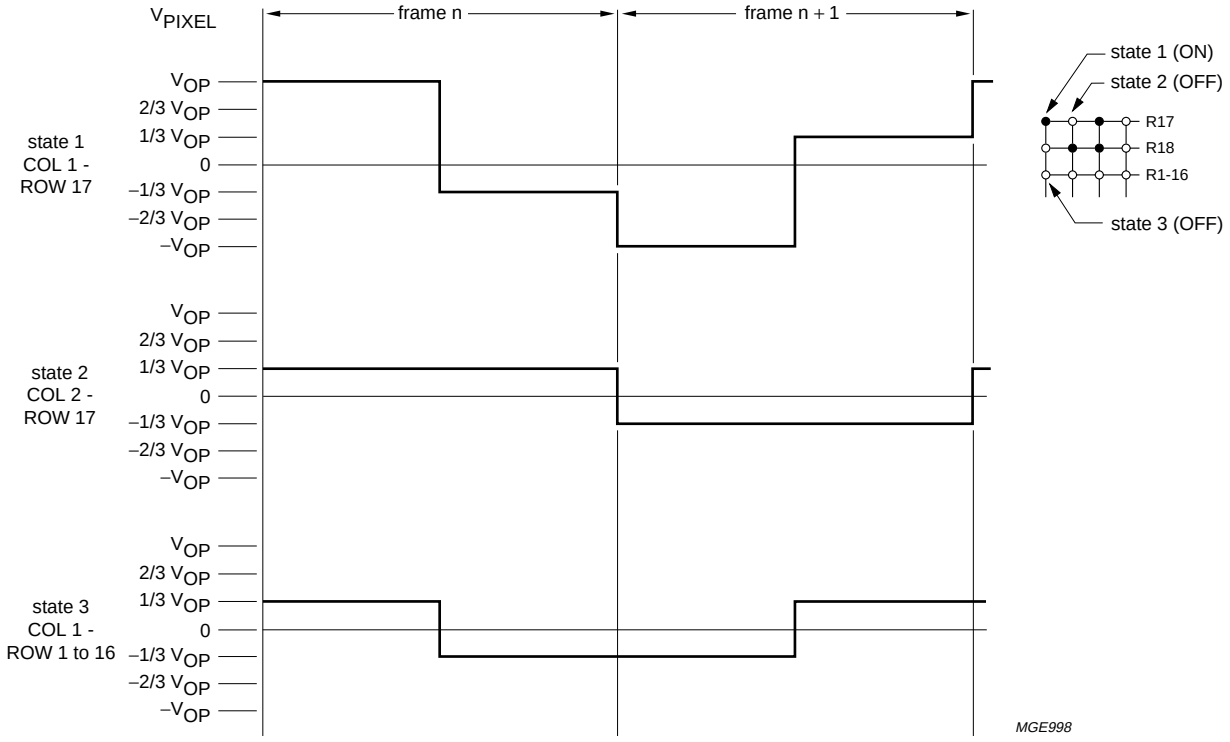


Fig.14 MUX 1 : 2 LCD waveforms; icon mode.



$V_{ON(rms)} = 0.745V_{OP}$

$V_{OFF(rms)} = 0.333V_{OP}$

$$D = \frac{V_{ON}}{V_{OFF}} = 2.23$$

Fig.15 MUX 1 : 2 LCD waveforms; icon mode.

7.16 Reset function

The PCF2113x automatically initializes (resets) when power is turned on. The chip executes a reset sequence, including a ‘clear display’, requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 3.

Table 3 State after reset

STEP	FUNCTION	CONTROL BIT STATE	CONDITIONS
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
		SL = 0	MUX 1 : 18 mode
5	default address pointer to DDRAM; the Busy Flag (BF) indicates the busy state (BF = 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 17 and 18		
6	icon control	IM = 0; IB = 0; DM = 0	icons, icon blink and direct mode disabled
7	display/screen configuration	L = 0; P = 0; Q = 0	default configurations
8	V_{LCD} temperature coefficient	TC1 = 0; TC2 = 0	default temperature coefficient
9	set V_{LCD}	V_A = 0; V_B = 0	V_{LCD} generator off
10	I^2C-bus interface reset		
11	Set HVgen stages	S1 = 1; S0 = 0	V_{LCD} generator voltage multiplier set at factor 4

8 INSTRUCTIONS

Only two PCF2113x registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers, to allow interfacing to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs.

The instruction set for I^2C-bus commands is given in Table 4.

The PCF2113x operation is controlled by the instructions shown in Table 5 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate PCF2113x functions such as display format, data length, etcetera.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instructions other than the ‘read busy flag’ and ‘read address’ instructions will be executed. Because the busy flag is set to a logic 1 while an instruction is being executed, check to ensure it is a logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 5. An instruction sent while the busy flag is logic 1 will not be executed.

Table 4 Instruction set for I^2C-bus commands

CONTROL BYTE								COMMAND BYTE								I^2C-BUS COMMANDS
Co	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	note 1

Note

1. R/$\overline{W}$ is set together with the slave address.

Table 5 Instruction set with parallel bus commands

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRE CLOCK CYCLES
H = 0 or 1												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	SL	H	sets interface Data Length (DL), number of display lines (M), single line/MUX 1 : 9 (SL) and extended instruction set control (H)	3
Read busy flag and address counter	0	1	BF	A_C							reads the Busy Flag (BF) indicating internal operating is being performed and reads Address counter (A_C) contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data from CGRAM or DDRAM	3
H = 0												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction (I/D) and specifies shift of display (S); these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D = 0 (display off) puts chip into the Power-down mode	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor or shifts display (S/C) to right or left (R/L) without changing DDRAM contents	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address; bit DB6 is to be set by the command ‘set DDRAM address’; look at the description of the commands	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRE CLOCK CYCLES
H = 1												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	–
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration (L)	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration, columns (P) and rows (Q)	3
Icon control	0	0	0	0	0	0	1	IM	IB	DM	set Icon Mode (IM), Icon Blink (IB), Direct Mode (DM)	3
Temperature control	0	0	0	0	0	1	0	0	TC1	TC2	set Temperature Coefficient (TCx)	3
Set HVgen stages	0	0	0	1	0	0	0	0	S1	S0	set internal V_{LCD} generator voltage multiplier stages (S1 = 1 and S0 = 1 not allowed)	3
Set V_{LCD}	0	0	1	V	voltage						store V_{LCD} in register V_A or V_B (V)	3

Table 6 Explanations of symbols used in Tables 4 and 5.

BIT	LOGIC STATE 0	LOGIC STATE 1
Co	last control byte; see Table 4	another control byte follows after data/command
DL	4 bits	8 bits
M (no impact, if SL = 1)	1-line by 24 display	2-line by 12 display
SL	MUX 1 : 18 (1 × 24 or 2 × 12 character display)	MUX 1 : 9 (1 × 12 character display)
H	use basic instruction set	use extended instruction set
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off; character at cursor position does not blink	cursor character blink on; character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
L (no impact, if M = 1 or SL = 1)	left/right screen: standard connection	left/right screen; mirrored connection
	1st 12 characters of 24; columns are from 1 to 60	1st 12 characters of 24; columns are from 1 to 60
	2nd 12 characters of 24; columns are from 1 to 60	2nd 12 characters of 24; columns are from 60 to 1
P	column data: left to right; column data is displayed from 1 to 60	column data; right to left; column data is displayed from 60 to 1
Q	row data; top to bottom; row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data; bottom to top; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	character mode; full display	icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
DM	direct mode disabled	direct mode enabled
V	set V_A	set V_B

8.1 Clear display

‘Clear display’ writes character code 20H into all DDRAM addresses (the character pattern for character code 20H must be a blank pattern), sets the DDRAM address counter to logic 0 and returns the display to its original position, if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction ‘clear display’ requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

8.2 Return home

‘Return home’ sets the DDRAM address counter to logic 0 and returns the display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

8.3 Entry mode set

8.3.1 BIT I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

8.3.2 BIT S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it appears as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM. When S = 0, the display does not shift.

8.4 Display control (and partial Power-down mode)

8.4.1 BIT D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting D = 1.

When the display is off (D = 0) the chip is in partial Power-down mode:

- The LCD outputs are connected to V_{SS}
- The LCD generator and bias generator are turned off.

Three oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards the oscillator can be stopped. If the oscillator is running during partial Power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure I_{DD} < 1 μA, the parallel bus pins DB7 to DB0 should be connected to V_{DD}; pins RS and R/$\overline{W}$ to V_{DD} or left open-circuit and pin PD to V_{DD}. Recovery from Power-down mode: PD back to V_{SS}, if necessary pin OSC back to V_{DD} and send a 'display control' instruction with D = 1.

8.4.2 BIT C

The cursor is displayed when C = 1 and inhibited when C = 0. Even if the cursor disappears, the display functions I/D, etcetera, remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.6).

8.4.3 BIT B

The character indicated by the cursor blinks when B = 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 second, with $f_{blink} = \frac{f_{OSC}}{52\,224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

8.5 Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor display shift'.

8.6 Function set

8.6.1 BIT DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open-circuit (internal pull-ups). Hence in the first 'function set' instruction after power-on M, SL and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set M, SL and H to their required values.

'Function set' from the I^2C-bus interface sets the DL bit to logic 1.

8.6.2 BIT M

Selects either 1-line by 24 display (M = 0) or 2-line by 12 display (M = 1).

8.6.3 BIT SL

Selects MUX 1 : 9, 1-line by 12 display (independent of M and L). Only rows 1 to 8 and 17 are to be used. All other rows must be left open-circuit. The DDRAM map is the same as in the 2-line by 12 display mode, however, the second line cannot be displayed.

8.6.4 BIT H

When H = 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

8.7 Set CGRAM address

'Set CGRAM address' sets bits DB5 to 0 of the CGRAM address A_{CG} into the address counter (binary A5 to A0). Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A6 to A0). With the 'set CGRAM address' command, only bits DB5 to DB0 are set. Bit DB6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write. All bits DB6 to DB0 can be read using the 'read busy flag' and 'read address' command.

When writing to the lower part of the CGRAM, ensure that bit DB6 of the address is not set (e.g. by an earlier DDRAM write or read action).

8.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address A_{DD} into the address counter (binary A6 to A0). Data can then be written to or read from the DDRAM.

8.9 Read busy flag and read address

'Read busy flag and address counter' read the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0. It is recommended that the BF status is checked before the next write operation is executed.

At the same time, the value of the address counter expressed in binary A6 to A0 is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

8.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data DB7 to DB0 to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits DB4 to DB0 of CGRAM data are valid, bits DB7 to DB5 are 'don't care'.

8.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data DB7 to DB0 from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while pin E is HIGH. After pin E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

There are only three instructions that update the data register:

- 'Set CGRAM address'
- 'Set DDRAM address'
- 'Read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display' and 'return home') do not modify the data register content.

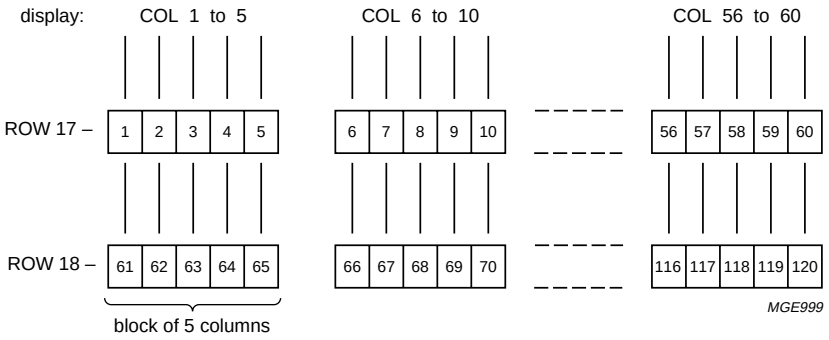
9 EXTENDED FUNCTION SET INSTRUCTIONS AND FEATURES

9.1 New instructions

H = 1 sets the chip into alternate instruction set mode.

9.2 Icon control

The PCF2113x can drive up to 120 icons. See Fig.16 for CGRAM to icon mapping.



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
56-60	even	17/56-60	0 0 0 0 0 0 0 1	0 0 0 1 0 1 1	1 1 1 1 1	
61-65	even	18/1-5	0 0 0 0 0 0 0 1	0 0 0 1 1 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	even	18/56-60	0 0 0 0 0 0 1 0	0 0 1 0 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	odd (blink)	18/56-60	0 0 0 0 0 1 1 0	0 1 1 0 0 1 1	0 0 1 1 0	

MGG001

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.
Data in character codes 0 to 3 define the icon state when icon blink is disabled or during the even phase when icon blink is enabled.
Data in character codes 4 to 7 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.16 CGRAM to icon mapping.

9.3 Bit IM

When IM = 0, the chip is in character mode. In the character mode characters and icons are driven (MUX 1 : 18). The V_{LCD} generator, if used, produces the V_{LCD} voltage programmed in register V_A.

When IM = 1, the chip is in icon mode. In the icon mode only the icons are driven (MUX 1 : 2) and the V_{LCD} generator, if used, produces the V_{LCD} voltage as programmed in register V_B.

Table 7 Normal/icon mode operation

IM	MODE	V_{LCD}
0	character mode	generates V_A
1	icon mode	generates V_B

9.4 Bit IB

Icon blink control is independent of the cursor/character blink function.

When IB = 0, the icon blink is disabled. Icon data is stored in CGRAM character 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons).

When IB = 1, the icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons). These bits also define icon state when icon blink is not used (see Table 9).

Icon states for the odd phase are stored in CGRAM character 4 to 6 (another 120 bits for the 120 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

9.5 Direct mode

When DM = 0, the chip is not in the direct mode. Either the internal V_{LCD} generator or an external voltage may be used to achieve V_{LCD}.

When DM = 1, the chip is in direct mode. The internal V_{LCD} generator is turned off and the V_{LCD2} output is directly connected to the V_{LCD} generator supply voltage V_{DD2}.

The direct mode can be used to reduce the current consumption when the required V_{LCD2} output voltage is close to the V_{DD2} supply voltage. This can be the case in icon mode or in Mux 1:9 (depending on LCD liquid properties).

9.6 Voltage multiplier control

Bits S1 and S0

A software configurable voltage multiplier is incorporated in the V_{LCD} generator and can be set via the ‘Set HVgen stages’ command.

The voltage multiplier control can be used to reduce current consumption by disconnecting internal voltage multiplier stages, depending on the required V_{LCD} output voltage (see Table 8).

Table 8 S1 and S0 control of voltage multiplier

S1	S0	DESCRIPTION
0	0	set V_{LCD} generator stages to 1 (2 x voltage multiplier)
0	1	set V_{LCD} generator stages to 2 (3 x voltage multiplier)
1	0	set V_{LCD} generator stages to 3 (4 x voltage multiplier)
1	1	do not use

9.7 Screen configuration

Bit L

L = 0: the two halves of a split screen are connected in a standard way i.e. column 1/61, 2/62 to 60/120; default.

L = 1: the two halves of a split screen are connected in a mirrored way i.e. column 1/120, 2/119 to 60/61. This allows single layer PCB or glass layout.

Table 9 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor character blink	block (all on)	normal (display character)
Icons	state 1; CGRAM character 0 to 2	state 2; CGRAM character 4 to 6

9.8 Display configuration

Bit P

P = 0: default.

P = 1: mirrors the column data.

Bit Q

Q = 0: default.

Q = 1: mirrors the row data.

9.9 Temperature control

Default is TC1 = 0 and TC2 = 0. Selects the default temperature coefficient for the internally generated V_{LCD} (see Table 10).

The ranges for TC are given in Chapter 13.

Table 10 TC1 and TC2 selection of V_{LCD} temperature coefficient

TC1	TC2	DESCRIPTION
0	0	V_{LCD} temperature coefficient 0
1	0	V_{LCD} temperature coefficient 1
0	1	V_{LCD} temperature coefficient 2
1	1	V_{LCD} temperature coefficient 3

9.10 Set V_{LCD}

The V_{LCD} value is programmed by instruction. Two on-chip registers, V_A and V_B hold V_{LCD} values for the character mode and the icon mode respectively. The generated V_{LCD} value is independent of V_{DD}, allowing battery operation of the chip.

V_{LCD} programming:

1. Send ‘function set’ instruction with H = 1
2. Send ‘set V_{LCD}’ instruction to write to voltage register:
   a) DB7, DB6 = 10: DB5 to DB0 are V_{LCD} of character mode (V_A)
   b) DB7, DB6 = 11: DB5 to DB0 are V_{LCD} of icon mode (V_B)
   c) DB5 to DB0 = 000000 switches V_{LCD} generator off (when selected)
   d) During ‘display off’ and power-down the V_{LCD} generator is also disabled.
3. Send ‘function set’ instruction with H = 0 to resume normal programming.

9.11 Reducing current consumption

Reducing current consumption can be achieved by one of the options given in Table 11.

When V_{LCD} lies outside the V_{DD} range and must be generated, it is usually more efficient to use the on-chip generator than an external regulator.

Table 11 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	Icon mode (control bit IM)
Display on	Display off (control bit D)
V_{LCD} generator operating	Direct mode
Any mode	power-down (PD pin)

10 INTERFACES TO MICROCONTROLLER

10.1 Parallel interface

The PCF2113x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required (see Chapter 6).

In 4-bit mode data is transferred in two cycles of 4 bits each using pins DB7 to DB4 for the transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second cycle. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction, see Figs 17 to 19 for examples of bus protocol.

In 4-bit mode, pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

10.2 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are the Serial Data line (SDA) and the Serial Clock Line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

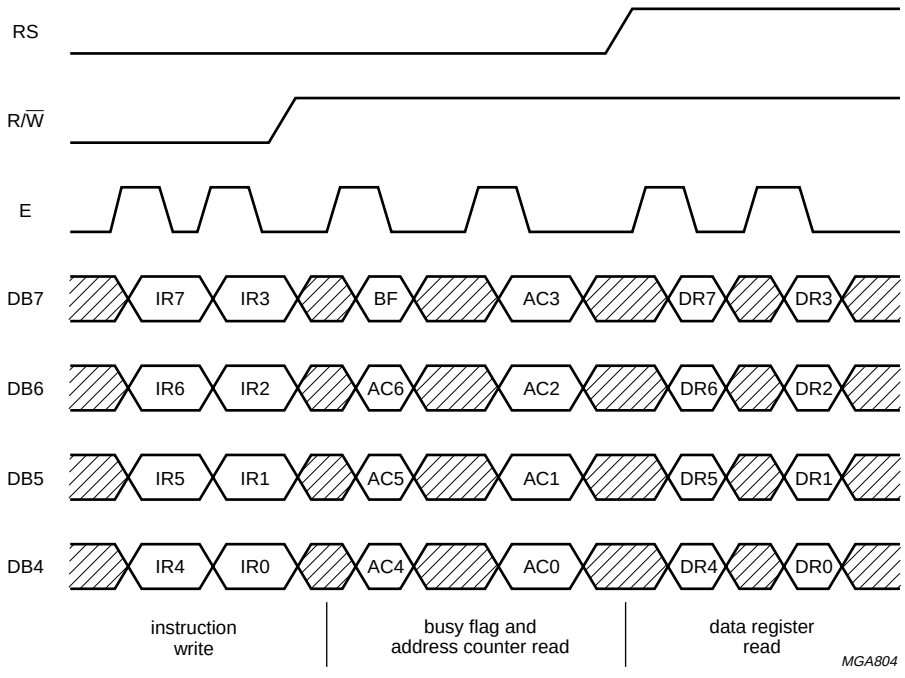
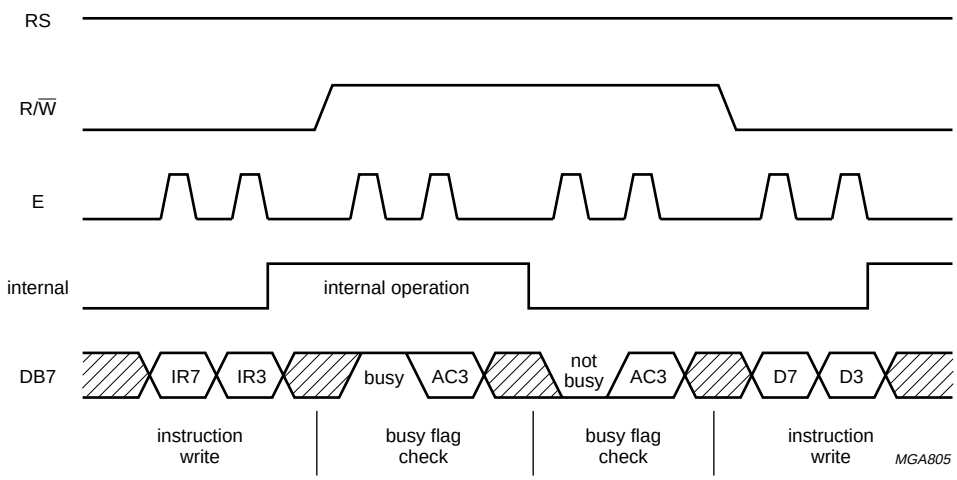


Fig.17 4-bit transfer example.



IR7, IR3: instruction 7th, 3rd bit.
AC3: address counter 3rd bit.
D7, D3: data 7th, 3rd bit.

Fig.18 An example of 4-bit data transfer timing sequence.

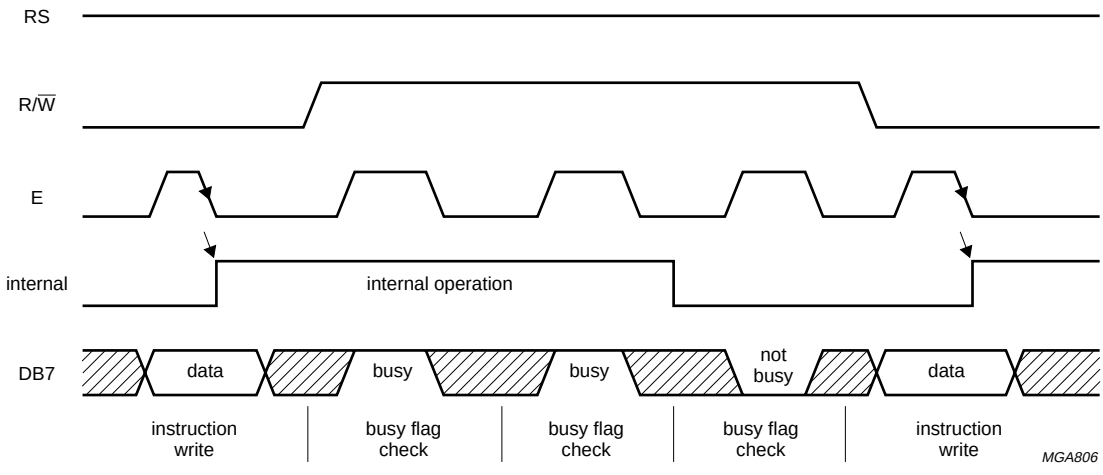


Fig.19 Example of busy flag checking timing sequence.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

10.2.1 I²C-BUS PROTOCOL

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The I²C-bus configuration for the different PCF2113x read and write cycles is shown in Figs 24 to 26. The slow down feature of the I²C-bus protocol (receiver holds SCL LOW during internal operations) is not used in the PCF2113x.

10.2.2 DEFINITIONS

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

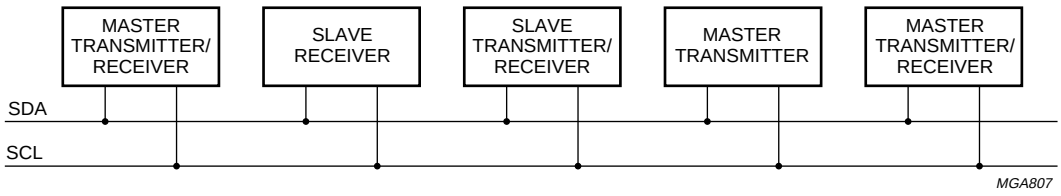


Fig.20 System configuration.

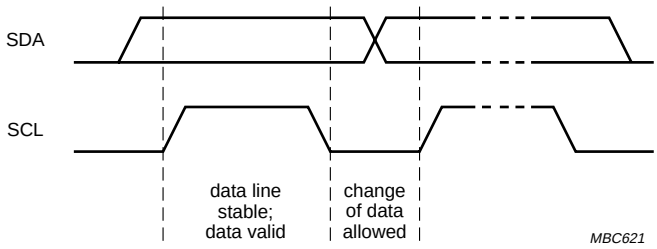


Fig.21 Bit transfer.

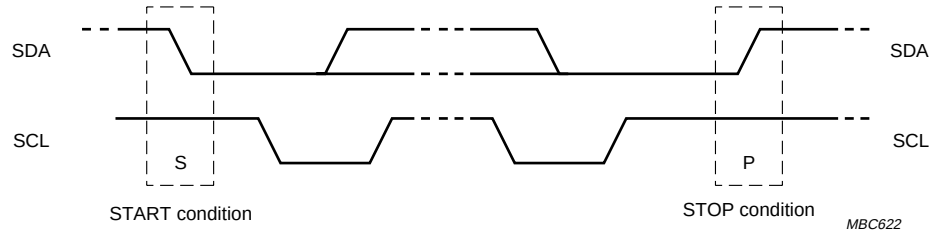


Fig.22 Definition of START and STOP conditions.

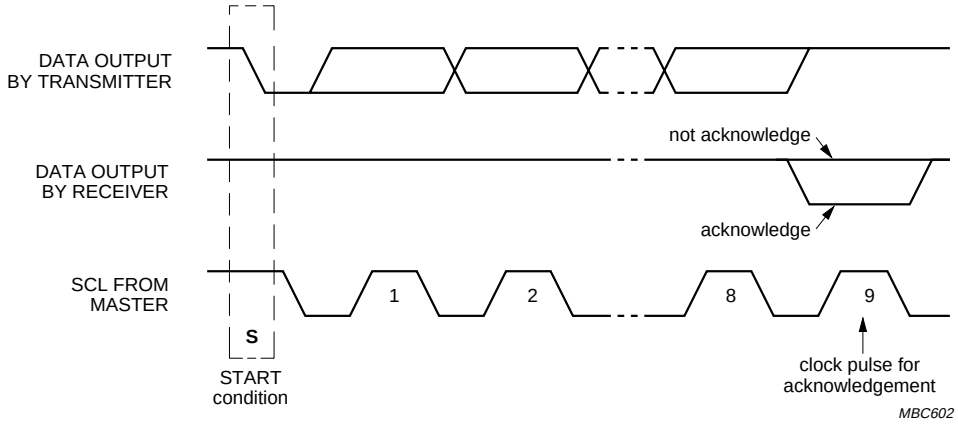


Fig.23 Acknowledgement on the I^2C-bus.

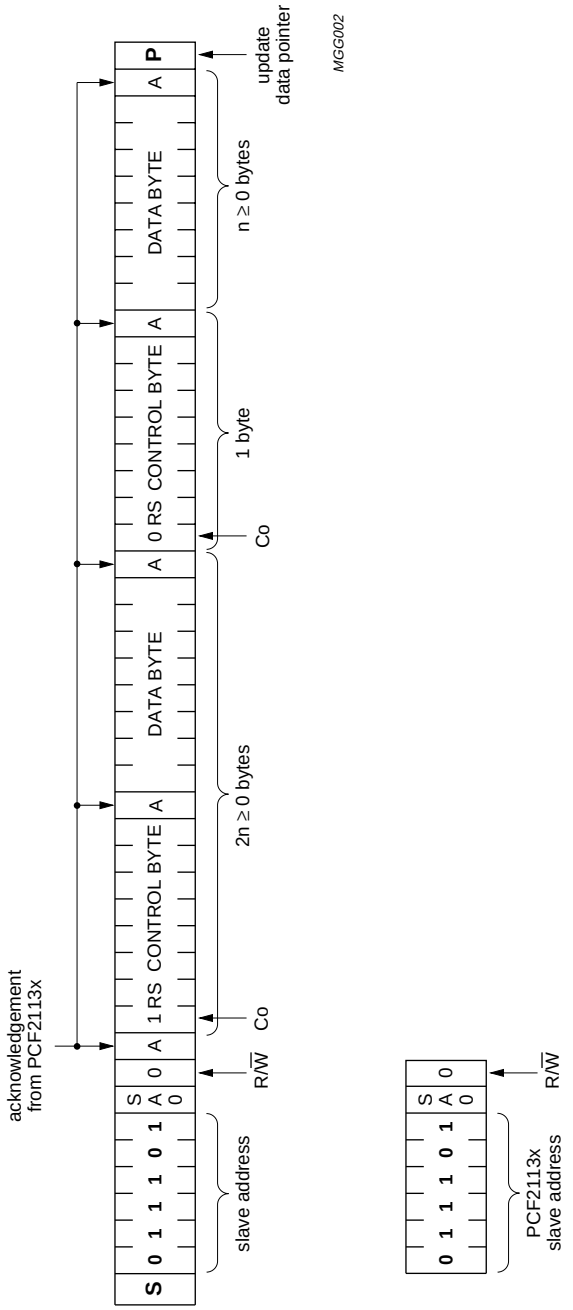
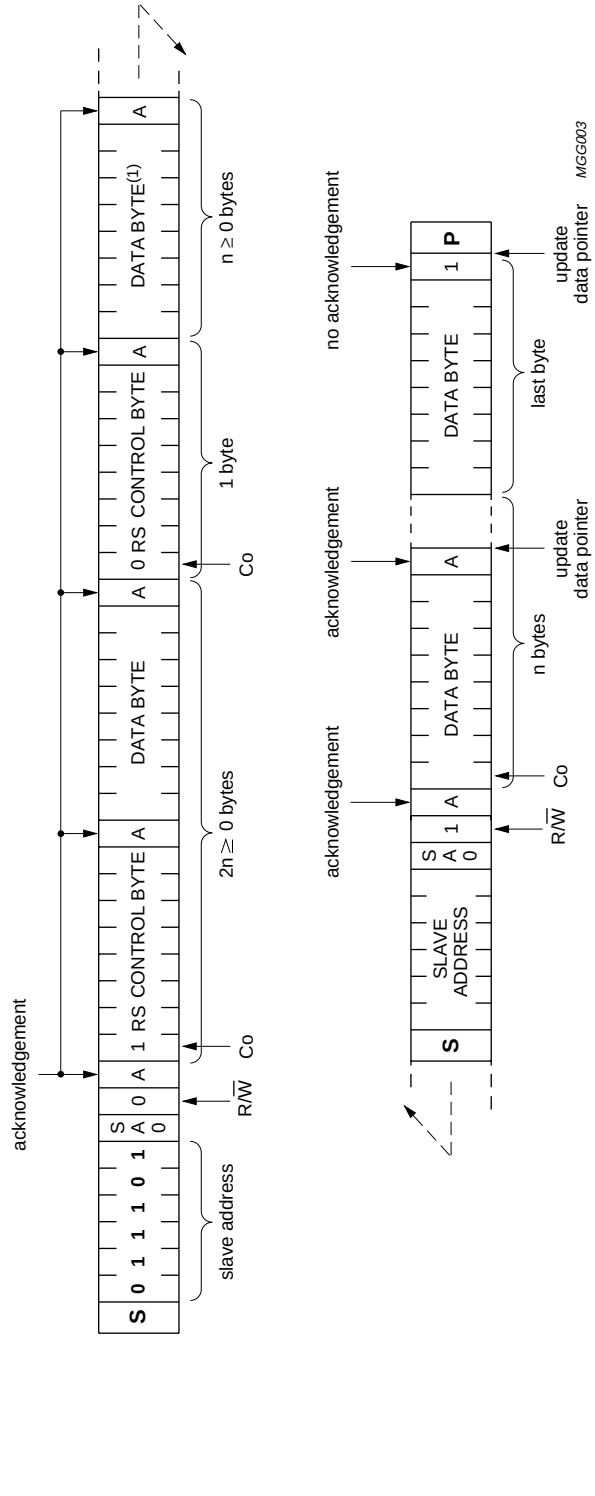


Fig.24 Master transmits to slave receiver; write mode.



Last data byte is a dummy byte (may be omitted).

Fig.25 Master reads after setting word address; writes word address, set RS; 'read data'.

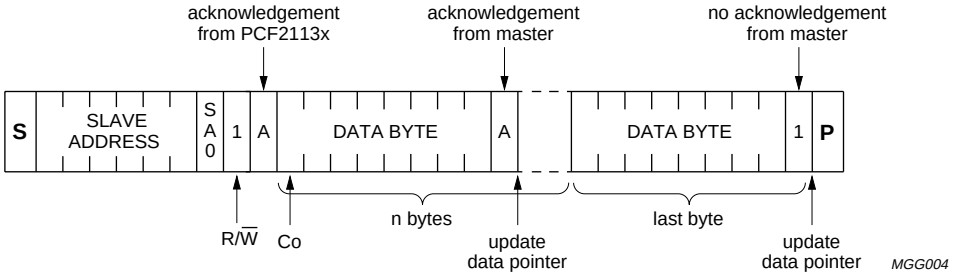


Fig.26 Master reads slave immediately after first byte; read mode (RS previously defined).

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD1}	logic supply voltage		–0.5	+5.5	V
V_{DD2}, V_{DD3}	V_{LCD} generator supply voltages		–0.5	+4	V
V_{LCD}	LCD supply voltage		–0.5	+6.5	V
$V_{i/o(n)}$	voltage on				
	any V_{DD} related input or output		–0.5	V_{DD} + 0.5	V
	any V_{LCD} related input or output		–0.5	V_{LCD} + 0.5	V
I_I	DC input current		–10	+10	mA
I_O	DC output current		–10	+10	mA
I_{DD}, I_{SS} and I_{LCD}	V_{DD}, V_{SS} or V_{LCD} supply current		–50	+50	mA
P_{tot}	total power dissipation		–	400	mW
P_O	power dissipation per output		–	100	mW
V_{es}	electrostatic handling voltage	human body model; C = 100 pF; R = 1.5 kΩ	–	2000	V
	electrostatic handling voltage	machine model; C = 200 pF; L = 0.75 μH	–	150	V
T_{stg}	storage temperature		–65	+150	°C

12 HANDLING INSTRUCTIONS

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

13 DC CHARACTERISTICS

V_{DD1} = 1.8 to 5.5 V; V_{DD2} = V_{DD3} = 2.2 to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD1}	logic supply voltage	note 1	1.8	–	5.5	V
V_{DD2}, V_{DD3}	V_{LCD} generator supply voltages	internal V_{LCD} generation (V_{DD2} and V_{DD3} < V_{LCD})	2.2	–	4.0	V
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
V_{POR}	Power-on reset voltage	note 1 and 2	0.9	–	1.6	V
GROUND SUPPLY CURRENT; EXTERNAL V_{LCD}; note 3						
I_{SS1}	ground supply current 1		–	70	120	µA
I_{SS3}	ground supply current 3	V_{DD} = 3 V; V_{LCD} = 5 V; note 4	–	45	80	µA
I_{SS4}	ground supply current 4	icon mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; note 4	–	25	45	µA
I_{SS5}	ground supply current 5	Power-down mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS and R/$\overline{W}$ = 1; OSC = 0; PD = 1	–	2	5	µA
GROUND SUPPLY CURRENT; INTERNAL V_{LCD}; notes 3 and 5						
I_{SS6}	ground supply current 6		–	190	400	µA
I_{SS8}	ground supply current 8	V_{DD} = 3 V; V_{LCD} = 5 V; note 4	–	160	400	µA
I_{SS9}	ground supply current 9	icon mode; V_{DD} = 2.5 V; V_{LCD} = 2.5 V; note 4	–	120	–	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS1}	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	V_{DD1}	V
$V_{IL(OSC)}$	LOW-level input voltage on pin OSC		V_{SS1}	–	V_{DD1} – 1.2	V
$V_{IH(OSC)}$	HIGH-level voltage pin OSC		V_{DD1} – 0.1	–	V_{DD1}	V
$I_{OL(DB)}$	LOW-level output current on pins DB7 to DB0	V_{OL} = 0.4 V; V_{DD1} = 5 V	1.6	4	–	mA
$I_{OH(DB)}$	HIGH-level output current on pins DB7 to DB0	V_{OH} = 4 V; V_{DD1} = 5 V	–1	–8	–	mA
I_{pu}	pull-up current at pins DB7 to DB0	V_I = V_{SS1}	0.04	0.15	1	µA
I_L	leakage current	V_I = V_{DD1} or V_{SS1}	–1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus; pins SDA and SCL						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	5.5	V
I_{LI}	input leakage current	$V_I = V_{DD1}$ or V_{SS1}	–1	–	+1	μA
C_i	input capacitance	note 6	–	5	–	pF
$I_{OL\ (SDA)}$	LOW-level output current on pin SDA	V_{OL} = 0.4 V; V_{DD1} > 2 V	3	–	–	mA
		V_{OL} = 0.2 V_{DD1}; V_{DD1} < 2 V	2	–	–	mA
LCD outputs						
$R_{O(ROW)}$	row output resistance of pins R1 to R18	note 7	–	10	30	kΩ
$R_{O(COL)}$	column output resistance of pins C1 to C60	note 7	–	15	40	kΩ
$V_{bias(tol)}$	bias voltage tolerance on pins R1 to R18 and C1 to C60	note 8	–	20	130	mV
$V_{LCD2(tol)}$	V_{LCD} voltage tolerance	T_{amb} = 25 °C; note 5				
		V_{LCD} < 3 V	–	–	160	mV
		V_{LCD} < 4 V	–	–	200	mV
		V_{LCD} < 5 V	–	–	260	mV
		V_{LCD} < 6 V	–	–	340	mV
TC0	V_{LCD} temperature coefficient 0		–	–0.16	–	%/K
TC1	V_{LCD} temperature coefficient 1		–	–0.18	–	%/K
TC2	V_{LCD} temperature coefficient 2		–	–0.21	–	%/K
TC3	V_{LCD} temperature coefficient 3		–	–0.24	–	%/K

Notes

1. Spikes on V_{DD1} or V_{SS1} which cause $V_{DD1} - V_{SS1} \leq 1.6$ V can cause a Power-on reset.
2. Resets all logic when $V_{DD1} < V_{POR}$; 3 OSC cycles required.
3. LCD outputs are open-circuit; inputs at V_{DD1} or V_{SS1}; bus inactive.
4. T_{amb} = 25 °C; f_{OSC} = 200 kHz.
5. LCD outputs are open-circuit; V_{LCD} generator is on; load current I_{VLCD} = 5 μA (at V_{LCD}).
6. Tested on sample basis.
7. Resistance of output pins (R1 to R18 and C1 to C60) with a load current of 10 μA; outputs measured one at a time; external V_{LCD} = 3 V, $V_{DD1, 2, 3}$ = 3 V.
8. LCD outputs open-circuit; external V_{LCD}.

14 AC CHARACTERISTICS

V_{DD1} = 1.8 to 5.5 V; V_{DD2} = V_{DD3} = 2.2 to 4.0 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	95	147	Hz
f_{osc}	oscillator frequency (not available at any pin)		140	250	450	kHz
$f_{OSC(ext)}$	external clock frequency		140	–	450	kHz
$t_{osc(st)}$	oscillator start-up time after power-down	note 1	–	200	300	µs
$t_{W(PD)}$	power-down HIGH-level pulse width		1	–	–	µs
$t_{SW(PD)}$	tolerable spike width on PD pin	note 1	–	–	90	ns
Timing characteristics of parallel interface; note 2						
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2113X); see Fig.27						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{su(D)}$	data set-up time		60	–	–	ns
$t_{h(D)}$	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2113X TO MICROCONTROLLER); see Fig.28						
$T_{cy(en)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{d(D)}$	data delay time	V_{DD1} > 2.2 V	–	–	150	ns
		V_{DD1} > 1.5 V	–	–	250	ns
$t_{h(D)}$	data hold time		5	–	100	ns
Timing characteristics of I^2C-bus interface; see Fig.29; note 2						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock LOW period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL and SDA rise time	note 1 and 3	15 + 0.1 C_b	–	300	ns
t_f	SCL and SDA fall time	note 1 and 3	15 + 0.1 C_b	–	300	ns
C_b	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns
t_{BUF}	bus free time between STOP and START condition		1.3	–	–	µs

Notes

1. Tested on sample base.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. C_b = total capacitance of one bus line in pF.

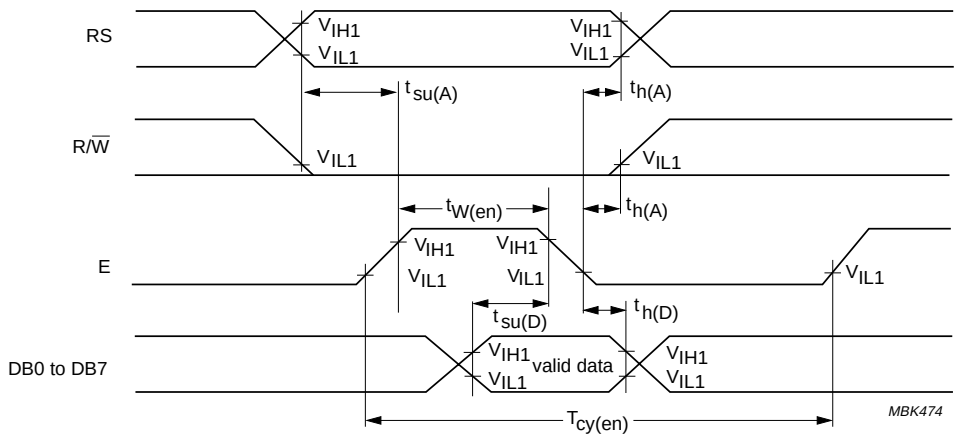


Fig.27 Parallel bus write operation sequence; writing data from microcontroller to PCF2113x.

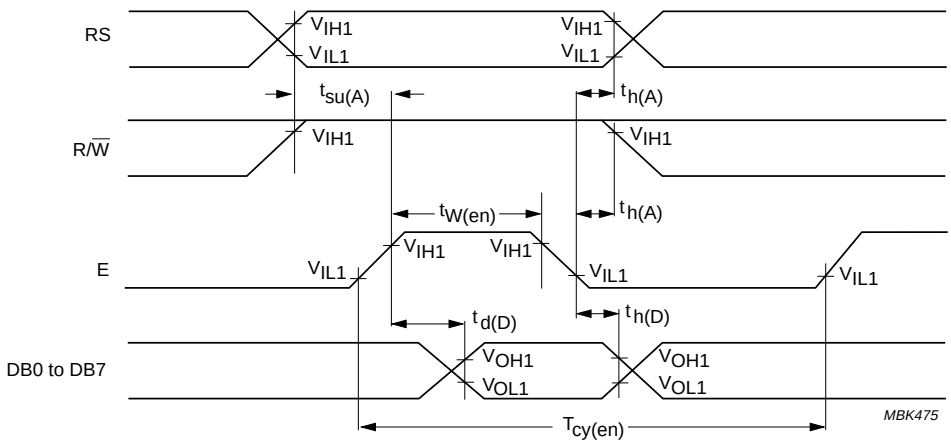


Fig.28 Parallel bus read operation sequence; writing data from PCF2113x to microcontroller.

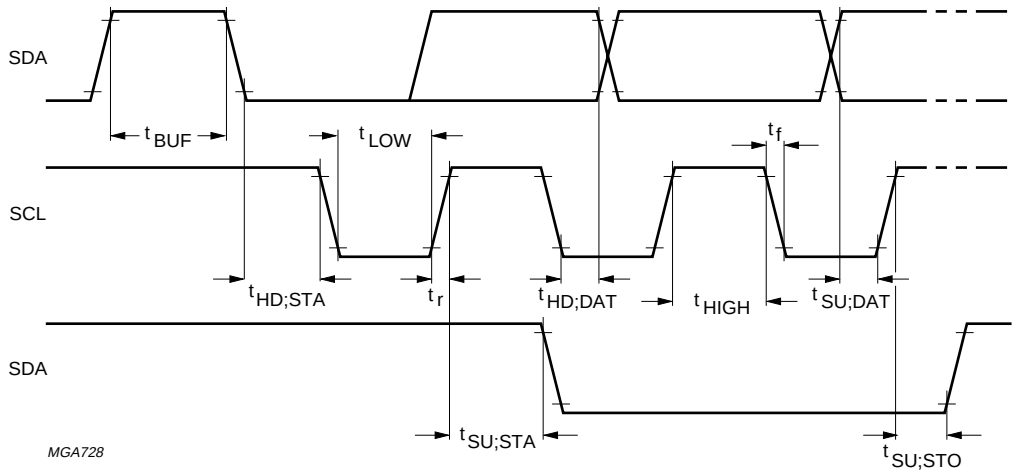
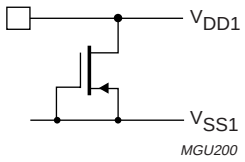
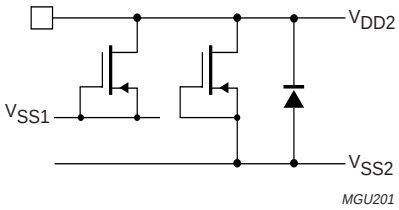
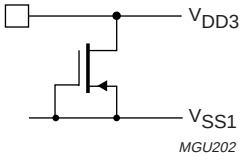
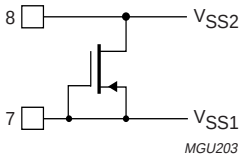
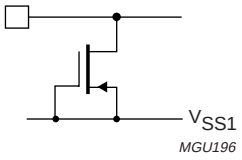
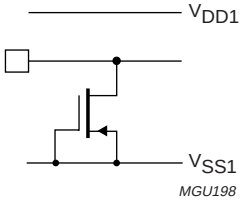
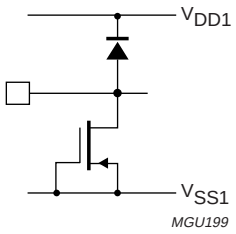
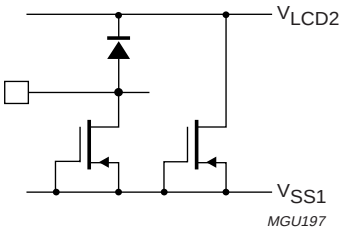


Fig.29 I²C-bus timing diagram.

15 DEVICE PROTECTION CIRCUITS

SYMBOL	PAD	INTERNAL CIRCUIT
V_{DD1}	1	
V_{DD2}	109	
V_{DD3}	110	
V_{SS1}	7	
V_{SS2}	8	
$V_{LCDSENSE}$	10	
V_{LCD1}	11	
V_{LCD2}	9	
SCL	96	
SDA	97	

SYMBOL	PAD	INTERNAL CIRCUIT
OSC	2	
PD	3	
T1	5	
T2	6	
T3	4	
E	98	
RS	99	
R/W	100	
DB0 to DB7	108 to 101	
R1 to R8	94 to 87	
R9 to R16	12 to 19	
R17	95	
R18	20	
C1 to C2	86 to 85	
C3 to 27	82 to 58	
C28 to C52	55 to 31	
C53 to C60	28 to 21	

16 APPLICATION INFORMATION

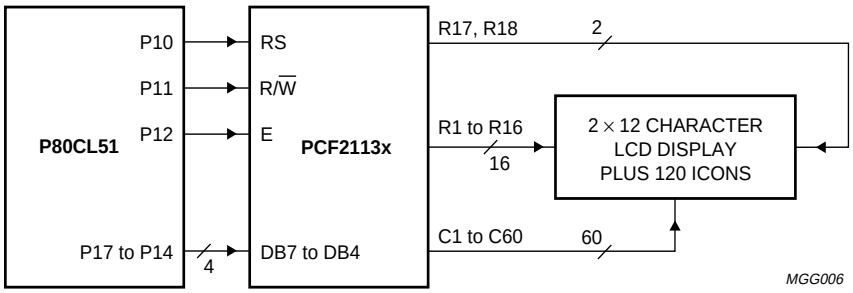


Fig.30 Direct connection to 8-bit microcontroller; 4-bit bus.

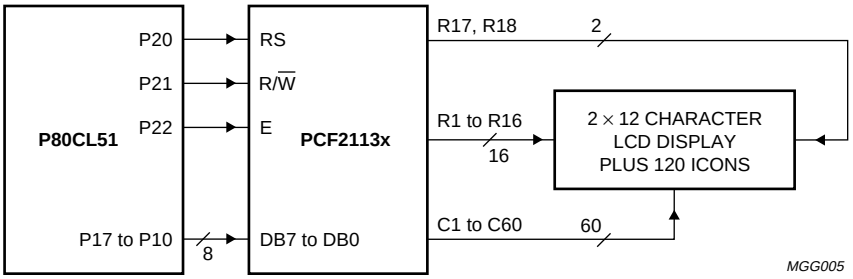


Fig.31 Direct connection to 8-bit microcontroller; 8-bit bus.

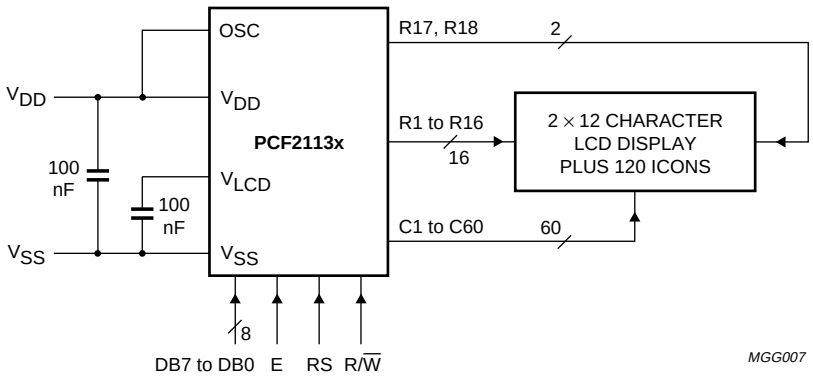


Fig.32 Typical application using parallel interface.

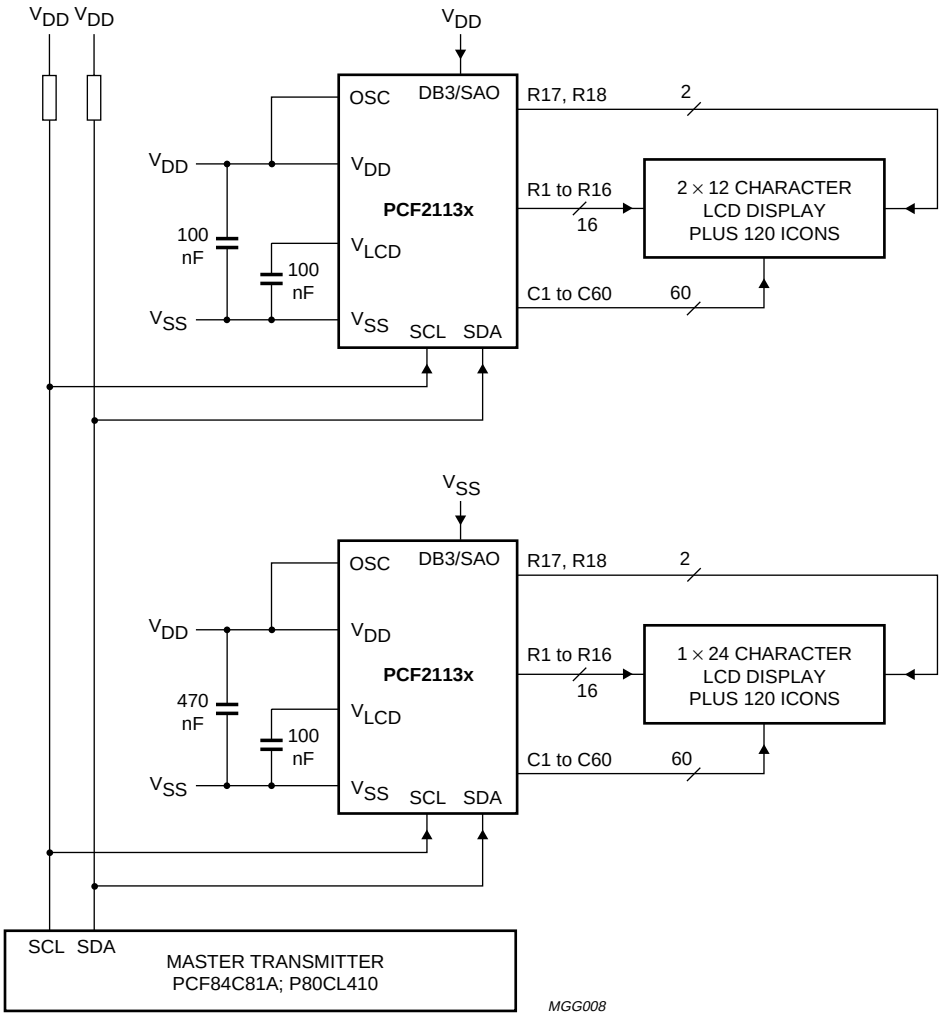


Fig.33 Application using I²C-bus interface.

16.1 General application information

The required minimum value for the external capacitors in an application with the PCF2113x are: C_{Ext} for V_{LCD}/V_{SS} = 100 nF min., for V_{DD}/V_{SS} = 470 nF. Higher capacitor values are recommended for ripple reduction.

For COG applications the recommended ITO track resistance is to be minimized for the I/O and supply connections.

Optimized values for these tracks are below 50 Ω for the supply and below 100 Ω for the I/O connections. Higher track resistance reduce performance and increase current consumption.

To avoid accidental triggering of Power-on reset (especially in COG applications), the supplies must be adequately decoupled. Depending on power supply quality, V_{DD1} may have to be risen above the specified minimum.

16.2 4-bit operation, 1-line display using internal reset

The program must set functions prior to a 4-bit operation (see Table 12). When power is turned on, 8-bit operation is automatically selected and the PCF2113x attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 12 step 3). Thus, DB4 to DB7 of the 'function set' are written twice.

16.3 8-bit operation, 1-line display using internal reset

Tables 13 and 14 show an example of a 1-line display in 8-bit operation. The PCF2113x functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and the DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

16.4 8-bit operation, 2-line display

For a 2-line display the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the 8th character is completed (see Table 15). It should be noted that both lines of the display are always shifted together; data does not shift from one line to the other.

16.5 I²C-bus operation, 1-line display

A control byte is required with most commands (see Table 16).

Table 12 4-bit operation, 1-line display example using internal reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2113x is initialized by the internal reset)							initialized; no display appears
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		sets to 4-bit operation; in this instance operation is handled as 8-bits by initialization and only this instruction completes with one write
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
	0	0	0	0	0	0		
4	display control							
	0	0	0	0	0	0	_	turns on display and cursor; entire display is blank after initialization
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM; display is not shifted
	0	0	0	1	1	0		
6	'write data' to CGRAM/DDRAM							
	1	0	0	1	0	1	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	0	0	0		

Table 13 8-bit operation, 1-line display example; using internal reset (character set ‘A’)

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2113x is initialized by the internal reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes ‘P’; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes ‘H’
7 to 10	|		writes ‘ILIP’
11	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes ‘S’
12	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	sets mode for display shift at the time of write
13	‘write data’ to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS** _	writes space
14	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M**_	writes ‘M’
15 to 19	|		writes ‘ICROK’
20	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**MICROKO**_	writes ‘O’

STEP	INSTRUCTION	DISPLAY	OPERATION
21	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
22	cursor/display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	shifts only the cursor position to the left
23	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1	**ICROCO**	writes ‘C’ correction; the display moves to the left
24	cursor/display shift 0 0 0 0 0 1 1 1 0 0	**MICROCO**	shifts the display and cursor to the right
25	cursor/display shift 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	shifts only the cursor to the right
26	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ICROCOM_**	writes ‘M’
27	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS M**	returns both display and cursor to the original position (address 0)

Table 14 8-bit operation, 1-line display and icon example; using internal reset (character set 'A')

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2113x is initialized by the internal reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	set CGRAM address 0 0 0 1 0 0 0 0 0 0	_	sets the CGRAM address to position of character 0; the CGRAM is selected
6	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon even phase; icons appears
7	| |		
8	set CGRAM address 0 0 0 1 1 1 0 0 0 0	_	sets the CGRAM address to position of character 4; the CGRAM is selected
9	'write data' to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon odd phase
10	| |		
11	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 1
12	icon control 0 0 0 0 0 0 1 0 1 0	_	icons blink
13	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 0

STEP	INSTRUCTION	DISPLAY	OPERATION
14	set DDRAM address 0 0 1 0 0 0 0 0 0 0		sets the DDRAM address to the first position; DDRAM is selected
15	'write data' to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes 'P'; the cursor is incremented by 1 and shifted to the right
16	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes 'H'
17 to 21	|		writes 'ILIPS'
22	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS**	returns both display and cursor to the original position (address 0)

Table 15 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2113x is initialized by the internal reset)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 1 0 0		sets to 8-bit operation; selects 2-line display and V_{LCD} generator off
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
5	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes ‘P’; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6 to 10	|		writes ‘HILIP’
11	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes ‘S’
12	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** **_**	sets DDRAM address to position the cursor at the head of the 2nd line
13	‘write data’ to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	writes ‘M’
14 to 18	|		writes ‘ICROC’
19	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**PHILIPS** **MICROCO**_	writes ‘O’

STEP	INSTRUCTION	DISPLAY	OPERATION
20	'write data' to CGRAM/DDRAM 0 0 0 0 0 0 0 1 1 1	**PHILIPS MICROCO_**	sets mode for display shift at the time of write
21	'write data' to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**HILIPS ICROCOM_**	writes 'M'; display is shifted to the left; the first and second lines shift together
23	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS MICROCOM**	returns both display and cursor to the original position (address 0)

Table 16 Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	I²C-BUS BYTE	DISPLAY	OPERATION
1	I²C-bus start		initialized; no display appears
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		during the acknowledge cycle SDA will be pulled-down by the PCF2113x
3	send a control byte for ‘function set’ Co RS 0 0 0 0 0 0 Ack 0 0 0 0 0 0 0 0 1		control byte sets RS for following data bytes
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
7	I²C-bus start	_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for ‘write data’ Co RS 0 0 0 0 0 0 Ack 0 1 0 0 0 0 0 0 1	_	
10	‘write data’ to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	**P**_	writes ‘P’; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right
11	‘write data’ to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH**_	writes ‘H’

STEP	I²C-BUS BYTE	DISPLAY	OPERATION
12 to 15	| |		
16	‘write data’ to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	writes ‘S’
17	(optional I²C-bus stop) I²C-bus start start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS_**	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I²C-bus start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I²C-bus interface to be shifted out; in the previous instruction neither a ‘set address’ nor a ‘read data’ has been performed; therefore the content of the DR was unknown; the R/W has to be set to 1 while still in I²C-write mode
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions
23	‘read data’: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	**PHILIPS**	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I²C-bus interface
24	‘read data’: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	**PHILIPS**	8 × SCL; code of letter ‘H’ is read first; during master acknowledge code of ‘I’ is loaded into the I²C-bus interface

STEP	I²C-BUS BYTE	DISPLAY	OPERATION
25	‘read data’: 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	**PHILIPS**	no master acknowledge; after the content of the I²C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register, data register is not updated, address counter is not incremented and cursor is not shifted
26	I²C-bus stop	**PHILIPS**	

Notes

1. X = don’t care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 17 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
					↓					
wait 2 ms after internal reset has been applied										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait 2 ms										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait more than 40 μs										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓ ↓					BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8 bits long); specify the number of display lines
0	0	0	0	1	1	0	M	0	H	
0	0	0	0	0	0	1	0	0	0	display off
0	0	0	0	0	0	0	0	0	1	clear display
0	0	0	0	0	0	0	1	I/D	S	entry mode set
					↓					
Initialization ends										

Note

1. X = don’t care.

Table 18 Initialization by instruction, 4-bit interface; not applicable for I^2C-bus operation

STEP						DESCRIPTION
power-on or unknown state						
			|			
Wait 2 ms after internal reset has been applied						
			|			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			|		
Wait 2 ms						
			|		
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			|		
Wait 40 μs						
			|		
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			|		BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bits long)
0	0	0	0	1	0	interface is 8 bits long
0	0	0	0	1	0	function set (interface is 4 bits long)
0	0	0	M	0	H	specify number of display lines
0	0	0	0	0	0	
0	0	1	0	0	0	display off
0	0	0	0	0	0	clear display
0	0	0	0	0	1	
0	0	0	0	0	0	entry mode set
0	0	0	1	I/D	S	
			|		
Initialization ends						

17 BONDING PAD INFORMATION

SYMBOL	PAD	COORDINATES(1)	
		X	Y
V_{DD1}	1	–1345	–1550
OSC	2	–1155	–1550
PD	3	–1055	–1550
T3	4	–845	–1550
T1	5	–765	–1550
T2	6	–665	–1550
V_{SS1}	7	–525	–1550
V_{SS2}	8	–455	–1550
V_{LCD2}	9	–295	–1550
$V_{LCDSENSE}$	10	–145	–1550
V_{LCD1}	11	+15	–1550
R9	12	+175	–1550
R10	13	+245	–1550
R11	14	+315	–1550
R12	15	+385	–1550
R13	16	+455	–1550
R14	17	+525	–1550
R15	18	+595	–1550
R16	19	+665	–1550
R18	20	+735	–1550
C60	21	+805	–1550
C59	22	+875	–1550
C58	23	+995	–1550
C57	24	+1065	–1550
C56	25	+1135	–1550
C55	26	+1205	–1550
C54	27	+1275	–1550
C53	28	+1345	–1550
dummy pad 1	29	+1435	–1550
dummy pad 2	30	+1630	–1395
C52	31	+1630	–1255
C51	32	+1630	–1155
C50	33	+1630	–1055
C49	34	+1630	–955
C48	35	+1630	–735
C47	36	+1630	–635
C46	37	+1630	–535
C45	38	+1630	–435
C44	39	+1630	–335
C43	40	+1630	–235
C42	41	+1630	–135
C41	42	+1630	–35
C40	43	+1630	+65
C39	44	+1630	+165
C38	45	+1630	+265
C37	46	+1630	+365
C36	47	+1630	+465
C35	48	+1630	+565
C34	49	+1630	+665
C33	50	+1630	+765
C32	51	+1630	+865
C31	52	+1630	+965
C30	53	+1630	+1065
C29	54	+1630	+1165
C28	55	+1630	+1265
dummy pad 3	56	+1630	+1335
dummy pad 4	57	+1435	+1550
C27	58	+1335	+1550
C26	59	+1225	+1550
C25	60	+1115	+1550
C24	61	+1005	+1550
C23	62	+765	+1550
C22	63	+665	+1550
C21	64	+565	+1550
C20	65	+465	+1550
C19	66	+365	+1550
C18	67	+265	+1550
C17	68	+165	+1550
C16	69	+65	+1550
C15	70	–35	+1550
C14	71	–135	+1550
C13	72	–235	+1550
C12	73	–335	+1550
C11	74	–435	+1550
C10	75	–535	+1550
C9	76	–635	+1550
C8	77	–735	+1550
C7	78	–835	+1550
C6	79	–965	+1550
C5	80	–1065	+1550
C4	81	–1165	+1550
C3	82	–1265	+1550
dummy pad 5	83	–1465	+1550
dummy pad 6	84	–1630	+1355
C2	85	–1630	+1255

SYMBOL	PAD	COORDINATES(1)	
		X	Y
C1	86	–1630	+1185
R8	87	–1630	+1115
R7	88	–1630	+1045
R6	89	–1630	+975
R5	90	–1630	+905
R4	91	–1630	+835
R3	92	–1630	+765
R2	93	–1630	+695
R1	94	–1630	+625
R17	95	–1630	+555
SCL	96	–1630	+375
SDA	97	–1630	+305
E	98	–1630	+85
RS	99	–1630	–15
R/W	100	–1630	–115

SYMBOL	PAD	COORDINATES(1)	
		X	Y
DB7	101	–1630	–215
DB6	102	–1630	–315
DB5	103	–1630	–415
DB4	104	–1630	–515
DB3	105	–1630	–615
DB2	106	–1630	–715
DB1	107	–1630	–815
DB0	108	–1630	–915
V_{DD2}	109	–1630	–1015
V_{DD3}	110	–1630	–1235
dummy pad 7	111	–1630	–1395
dummy pad 8	112	–1465	–1550

Note

1. All x and y coordinates are referenced to centre of chip and dimensions are in μm (see Fig.34).

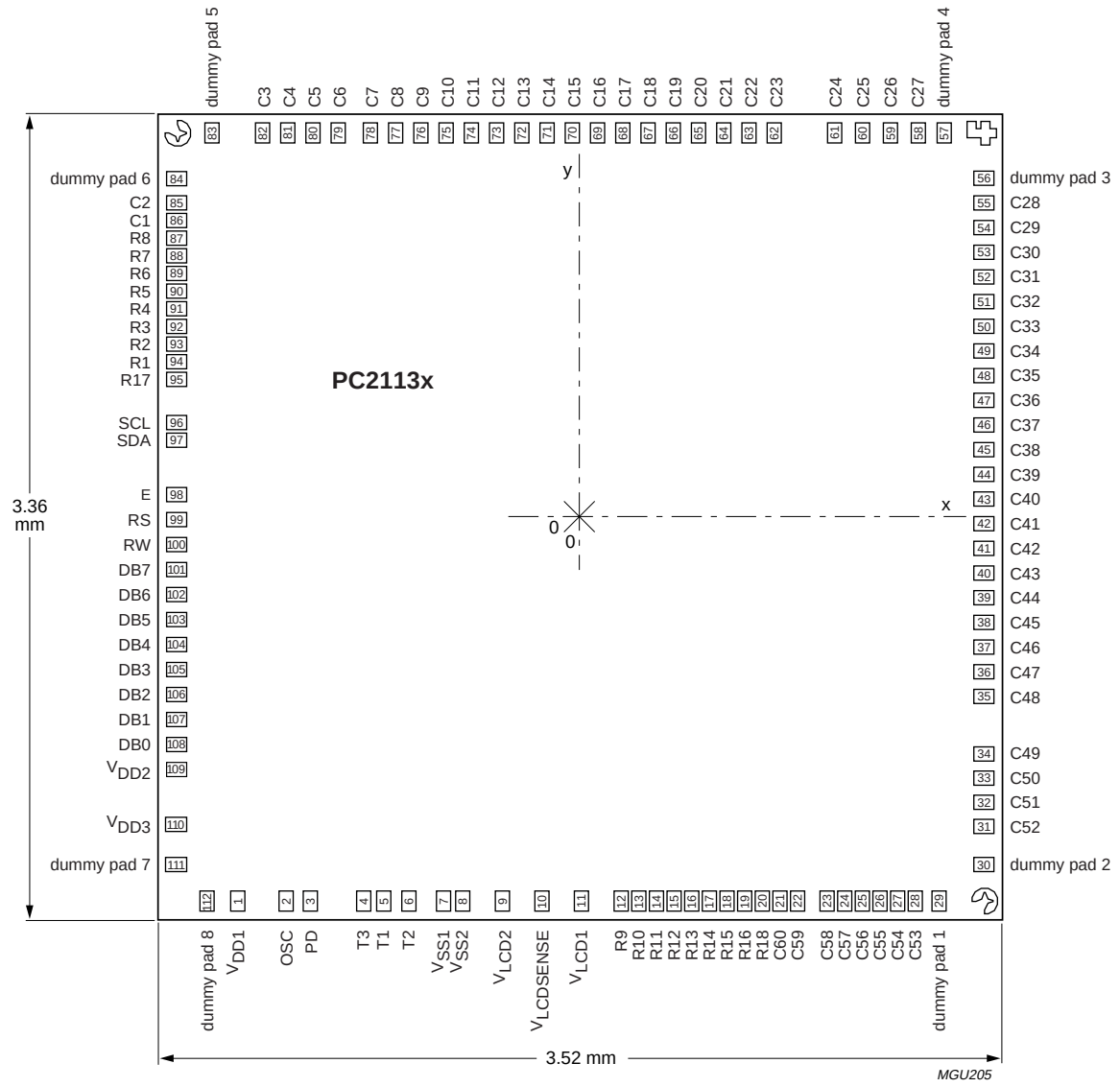
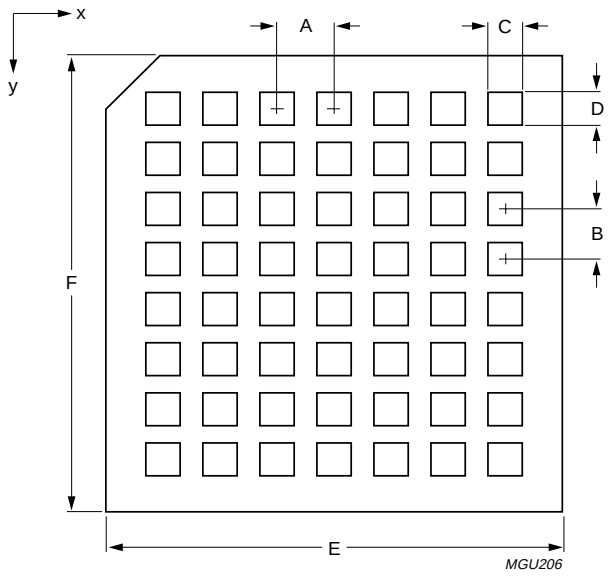


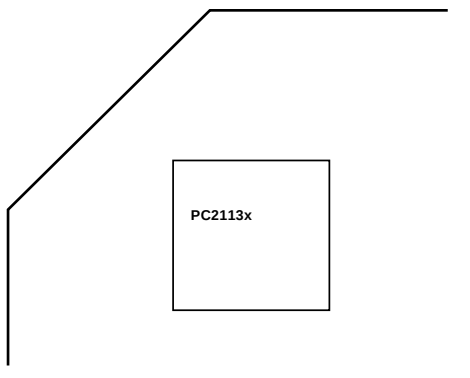
Fig.34 Bonding pad locations.

18 TRAY INFORMATION



For dimensions see Table 19.

Fig.35 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.36 Tray alignment.

Table 19 Tray dimensions

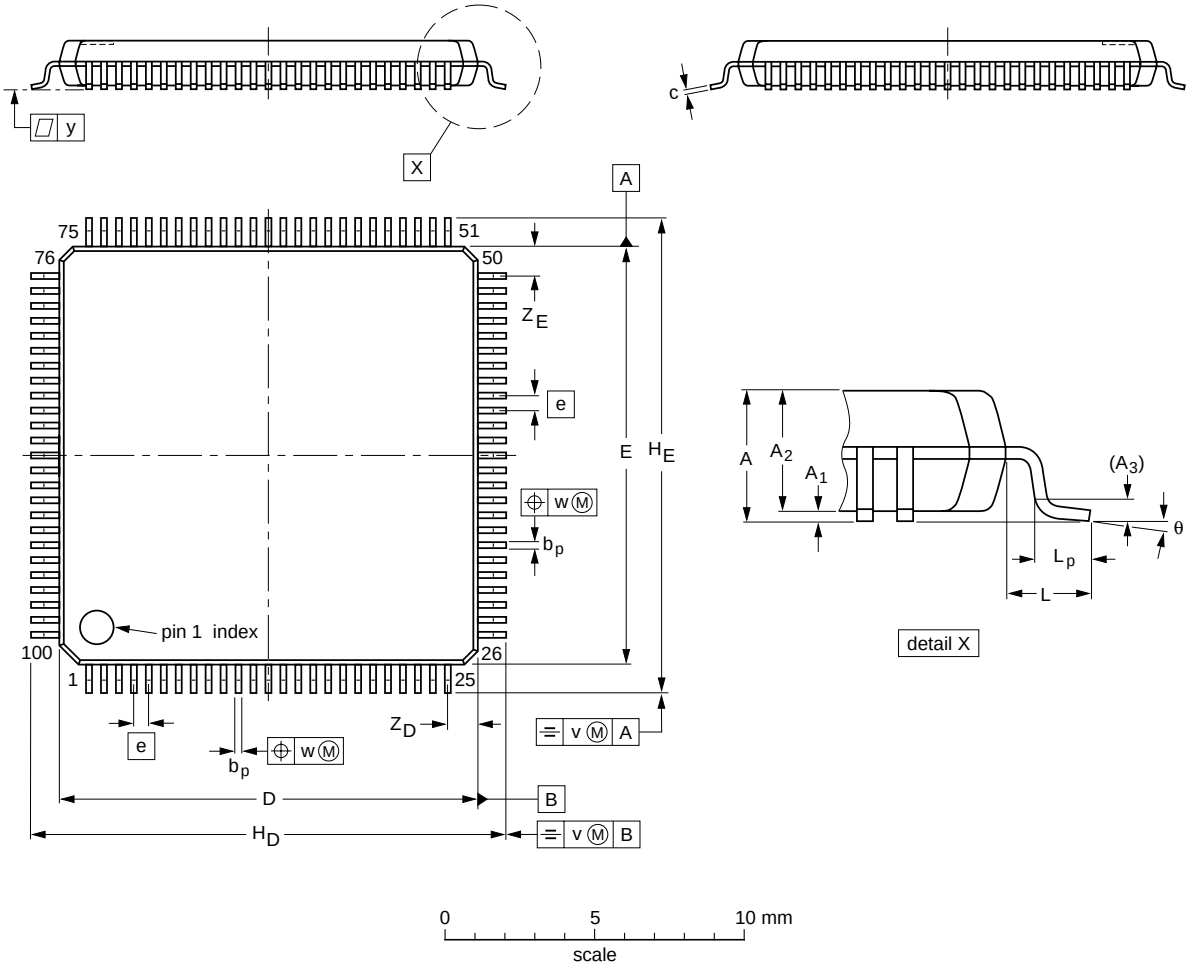
DIMENSION	DESCRIPTION	VALUE
A	pocket pitch x direction	6.35 mm
B	pocket pitch y direction	5.59 mm
C	pocket width x direction	3.82 mm
D	pocket width y direction	3.66 mm
E	tray width x direction	50.8 mm
F	tray width y direction	50.8 mm
x	pockets in x direction	7
y	pockets in y direction	8

Table 20 Bump size

PARAMETER	VALUE	UNIT
Type	galvanic pure Au	–
Bump width	50 ±6	µm
Bump length	90 ±6	µm
Bump height	17.5 ±5	µm
Height difference in one die	<2	µm
Convex deformation	<5	µm
Pad size, aluminium	62 × 100	µm
Passivation opening CBB	36 × 76	µm
Wafer thickness	380 ±25	µm

19 PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1	136E20	MS-026				~~00-01-19~~ 00-02-01

20 SOLDERING

20.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

20.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

20.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

20.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

20.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

21 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

22 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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